[illegible]

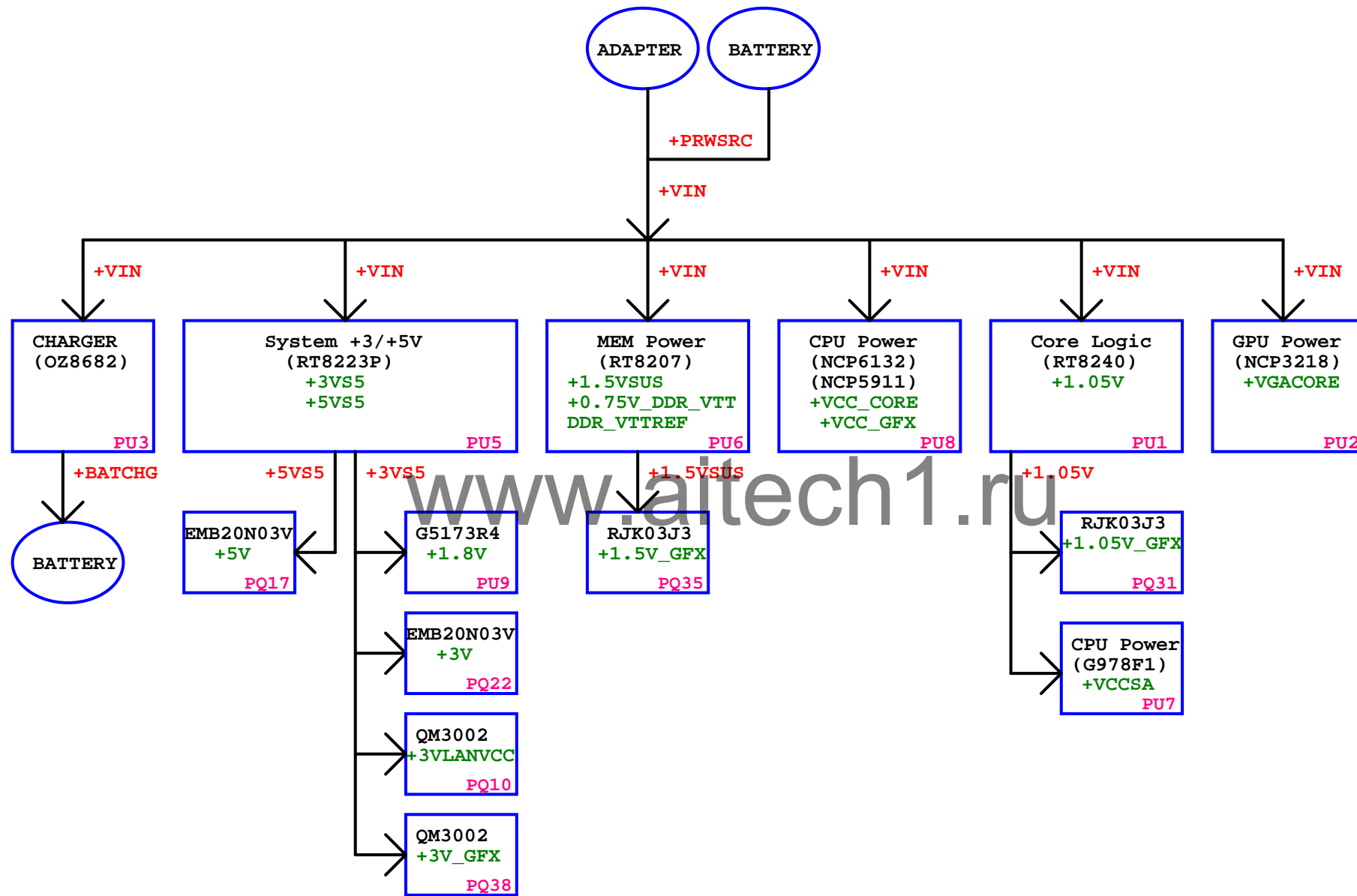
USB Master	Port Assignment
USB0	External port#1 (USB3.0)
USB1	External port#2 (USB3.0)
USB2	Camera
USB3	External port#3 (USB3.0)
USB4	NC
USB5	NC
USB6	NC
USB7	NC
USB8	NC
USB9	Debug
USB10	WLAN
USB11	NC
USB12	Touch Screen
USB13	NC

SATA Master	Port Assignment
SATA0	HDD
SATA1	mSATA
SATA2	NC
SATA3	NC
SATA4	NC
SATA5	NC

PCIE Master	Port Assignment
PCIE 1	WLAN
PCIE 2	LAN
PCIE 3	Card reader
PCIE 4	NC
PCIE 5	NC
PCIE 6	NC
PCIE 7	NC
PCIE 8	NC

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Main Power tree



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	Power Tree	3A
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Chief River mainly Power On Sequence(G3 to S0)

From Coin Cell BAT

VCCRTC

From AC,BATT

VIN

Sys +3v/+5v VR internal power

+5VPCU/ +3VPCU

From PW On Button to EC

NBSWON#

EC Assert S5_On when received NBSWON#

S5_ON

From EC(S5_ON) to System +3V/+5V PWM

+3VS5/+5VS5

From EC to PCH

EC_RSMRST#

From EC to PCH

DNBSWON#

PCH assert SUSCLK

SUSCLK

SUSCLK RUNNING

From PCH to EC

SUSB#/SUSC#

PCH Asserted SUSB#/SUSC# to EC to assert SUSON..

EC Assert SUS_ON

SUS_ON

SUSON Power rail

+1.5VSUS

EC Assert LAN_POWERON

LAN_POWERON

EC Assert MAIN_ON

MAIN_ON

MainOn Power Rails

+3V/+5V/+1.05V/+1.8V/+1.05V_VTT

1.05V_VTT_PWRGD to enable +VCCSA

1.05V_VTT_PWRGD

EC Received HW_PG
from MainOn/SUSON/VCCSA PowerGD

HW_PG

EC Assert VR_ON

VR_ON

EC defined 105ms from HWPG to VRON

EC Assert EC_PWROK

EC_PWROK(PCH_PWROK)

EC defined 125ms from HWPG to ECPWROK

IMVP_PWRGD to PCH SYS_PWROK

IMVP_PWRGD(PCH_SYS_PWROK)

DRAMPWROK DRAMPWROK

PCH assert UNCOREPWRGOOD to CPU

H_POWERGD

PCH Assert PLTRST#

PLTRST#

DMI

DMI_BUS

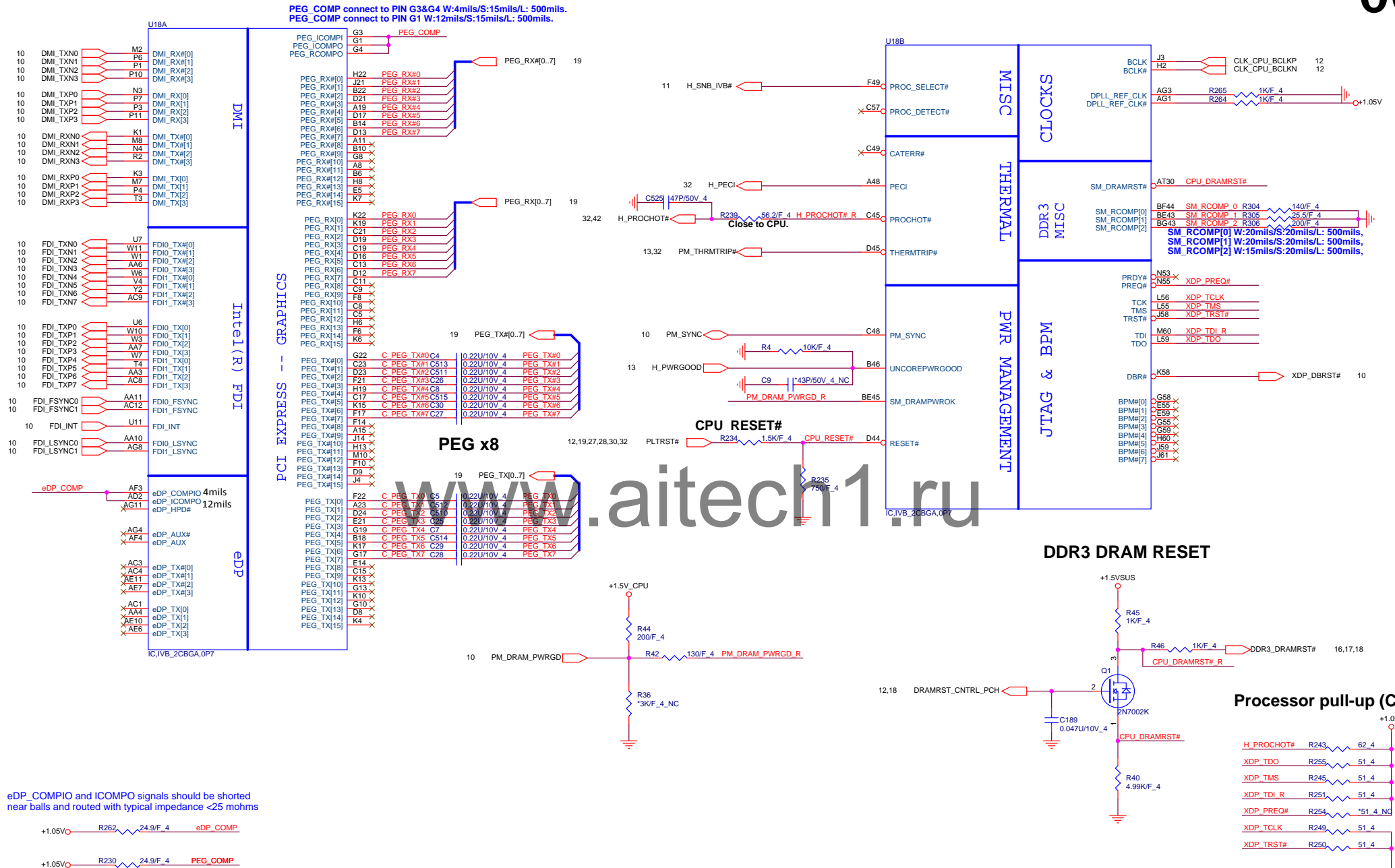
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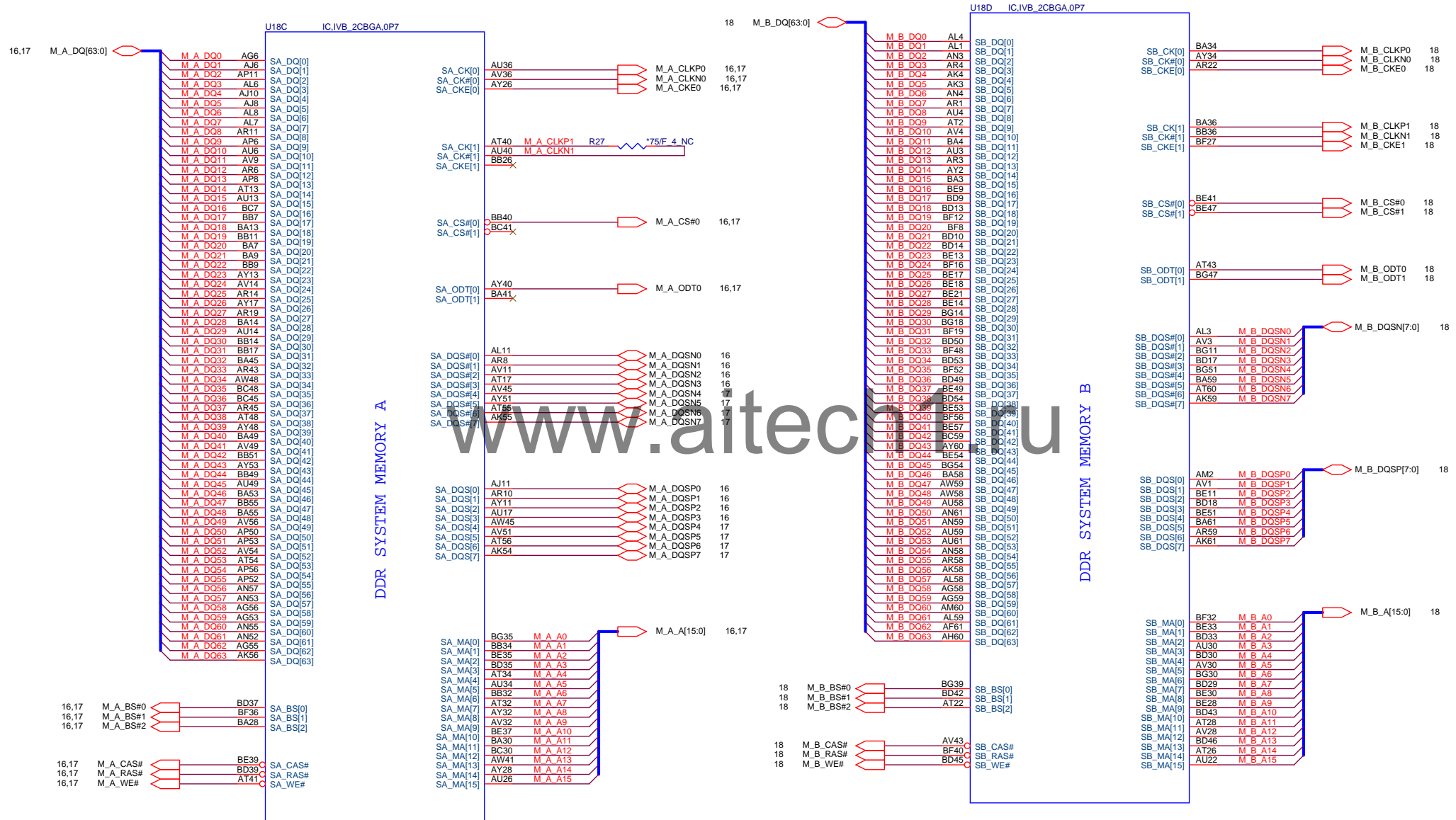
PROJECT : JW8

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Ivy Bridge Processor (DDR3)

07

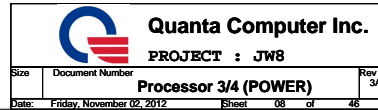


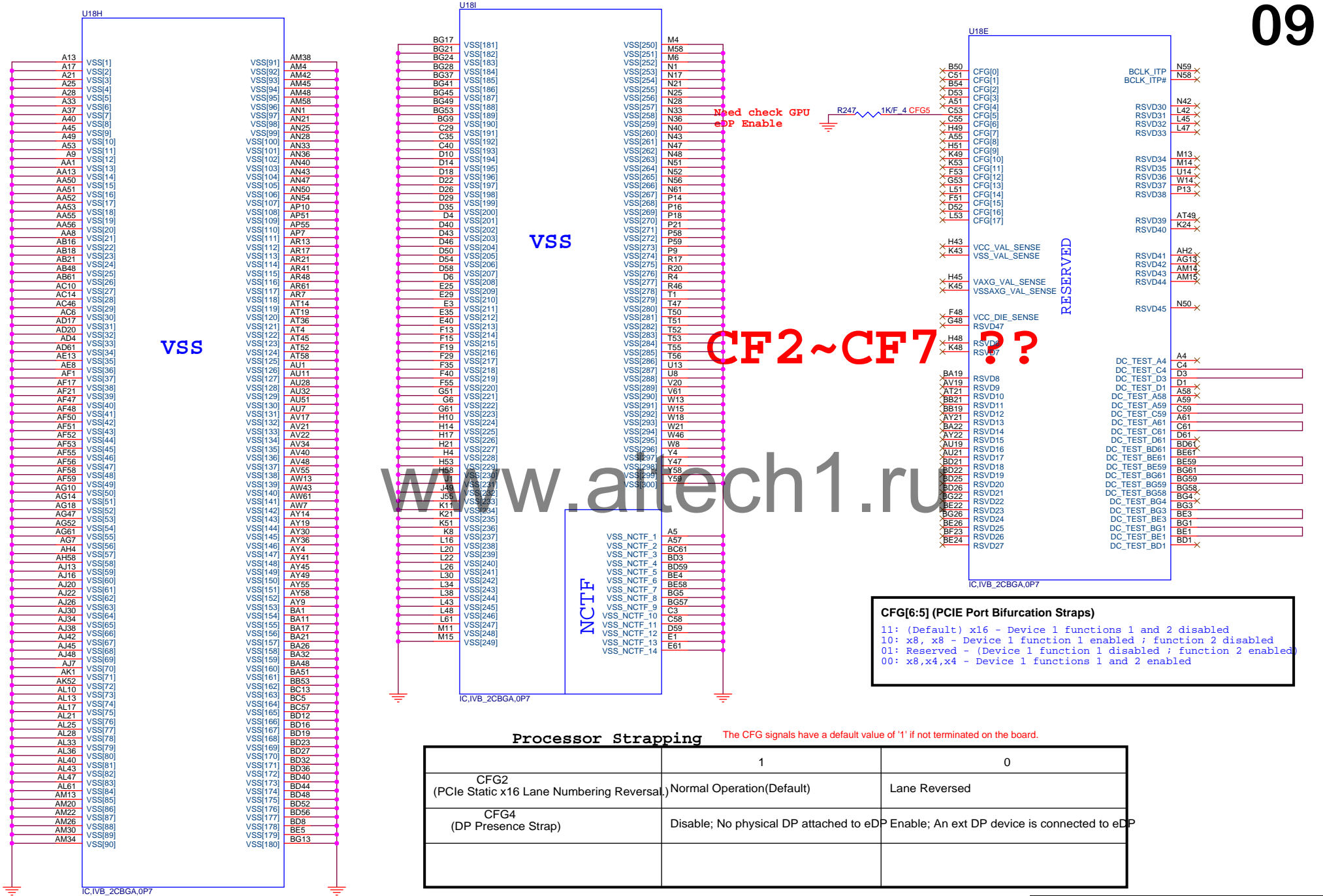
Quanta Computer Inc.

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Processor 2/5 (DDR3 I/F)





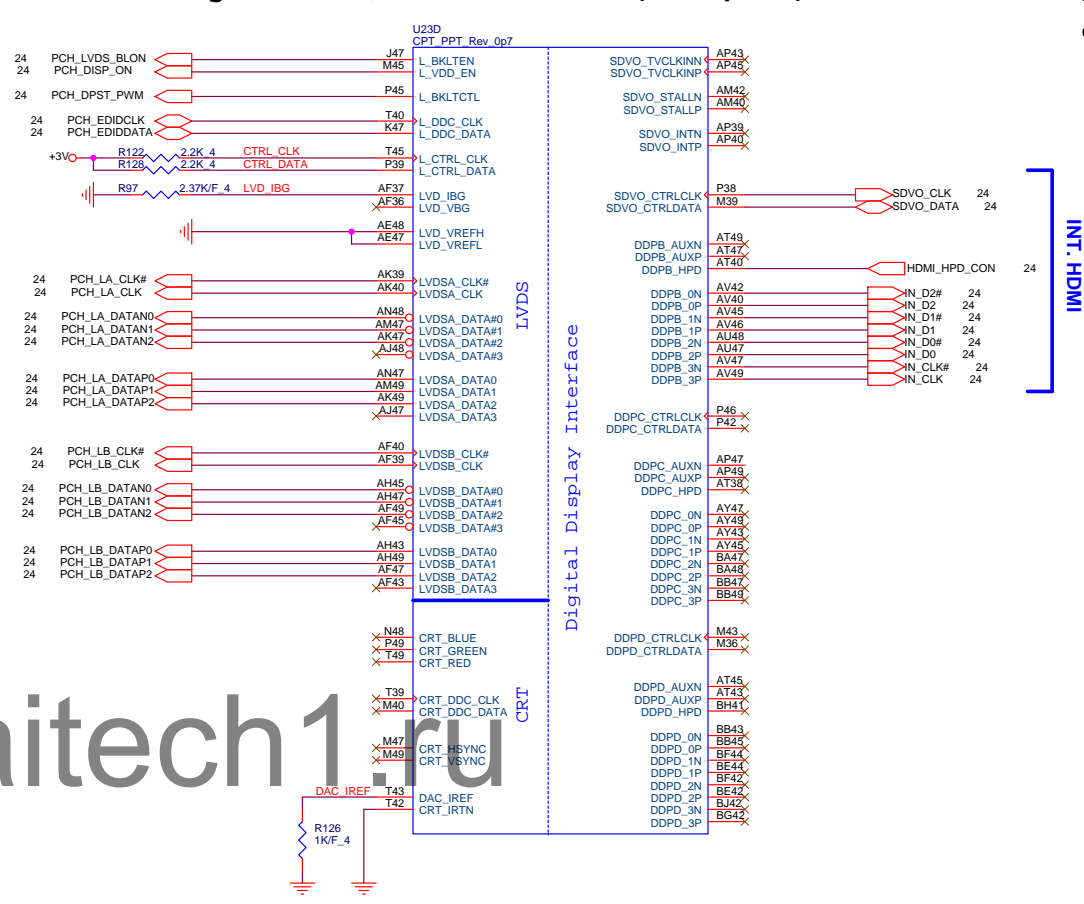
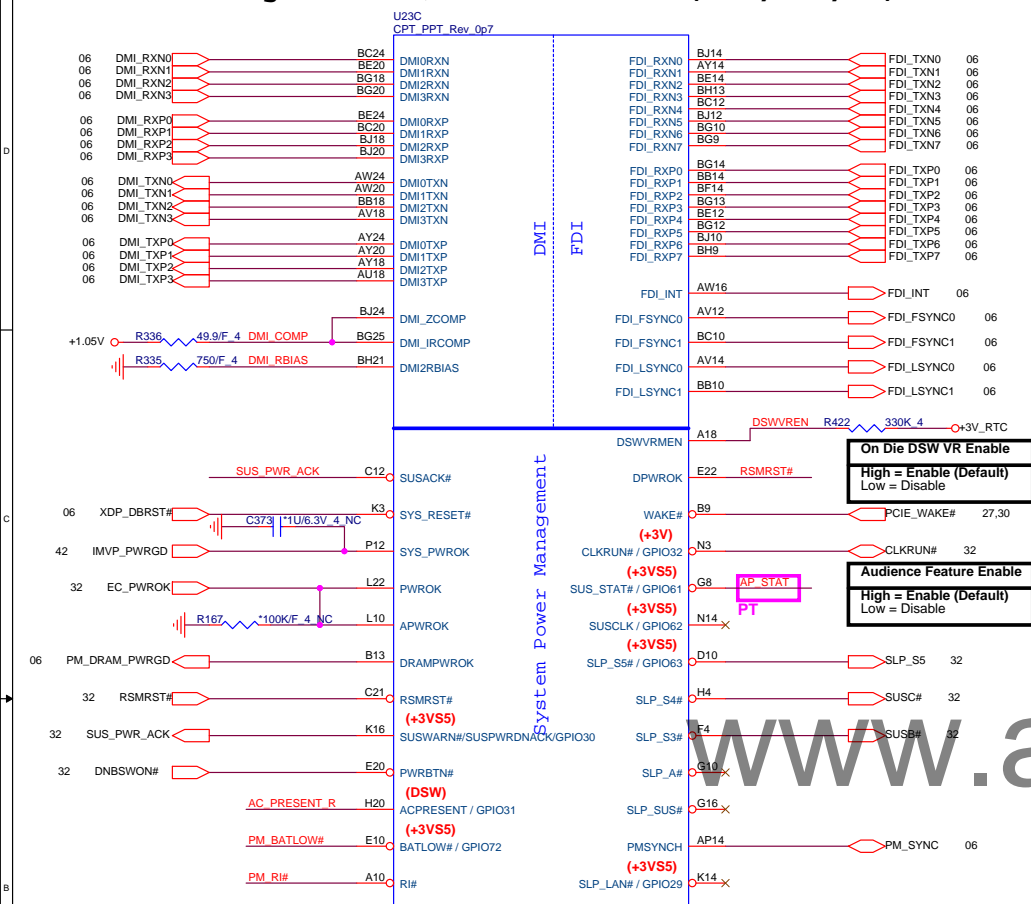
Processor Strapping		
	1	0
CFG2 (PCIe Static x16 Lane Numbering Reversal)	Normal Operation(Default)	Lane Reversed
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP Enable; An ext DP device is connected to eDP	

CFG[6:5] (PCIe Port Bifurcation Straps)

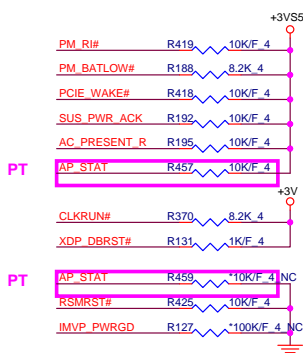
11: (Default) x16 - Device 1 functions 1 and 2 disabled
 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled
 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled)
 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled

Cougar Point/Panther Point (DMI,FDI,PM)

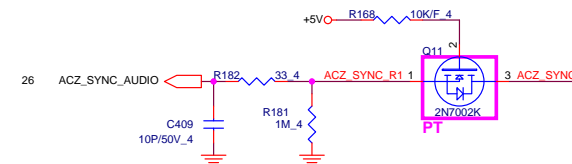
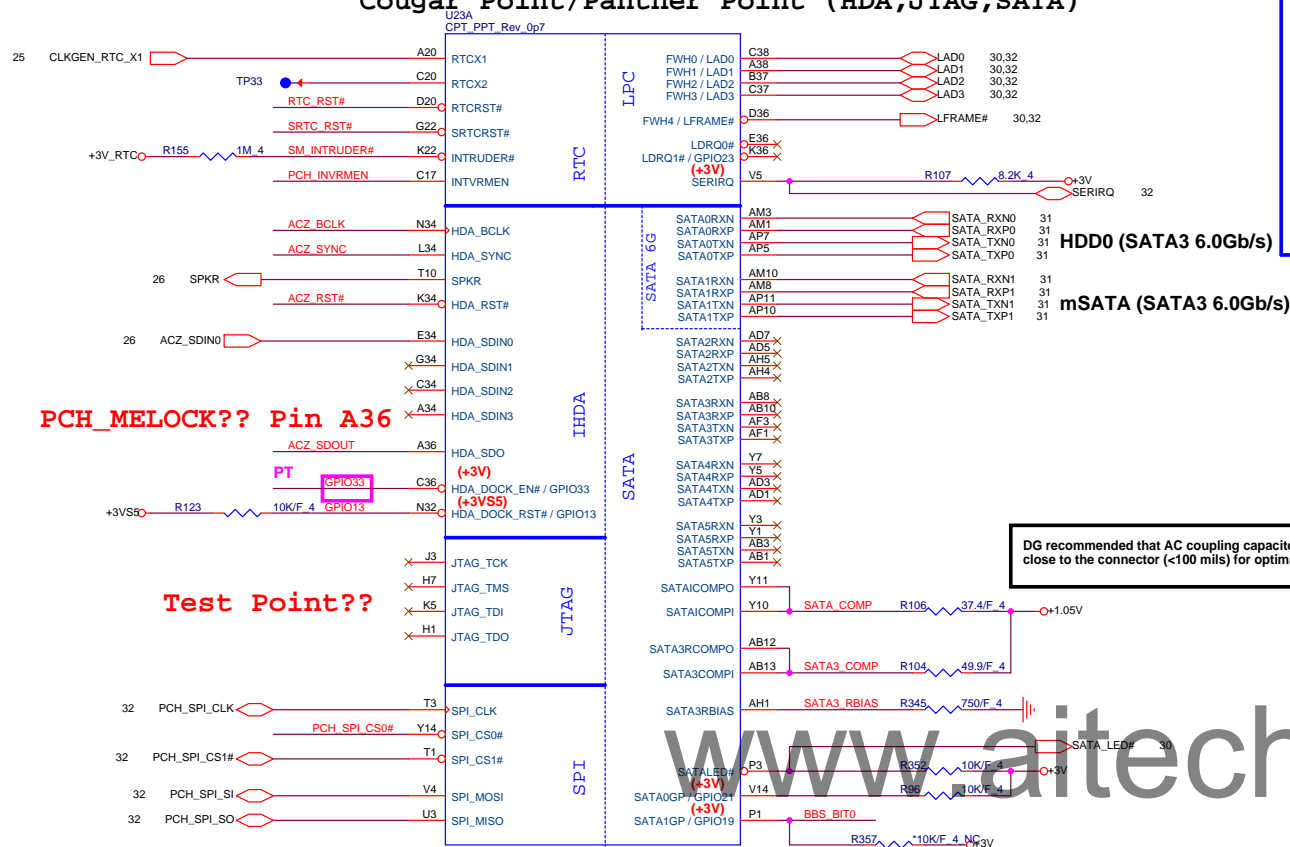
Cougar Point/Panther Point (LVDS,DDI)



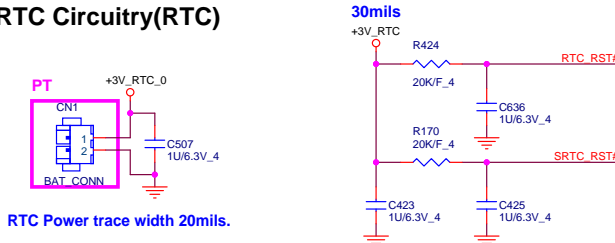
PCH Pull-high/low(CLG)



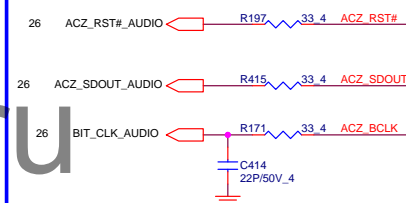
Cougar Point/Panther Point (HDA,JTAG,SATA)



RTC Circuitry(RTC)

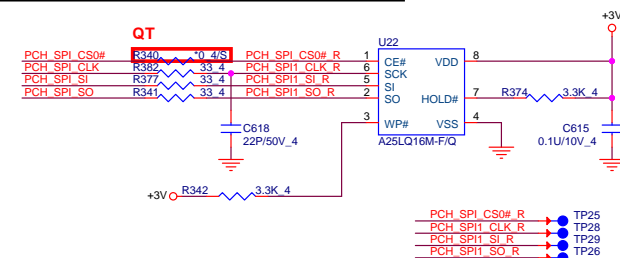


HDA Bus(CLG)










PCH SPI ROM(CLG)

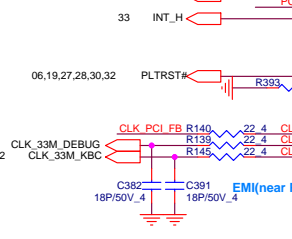
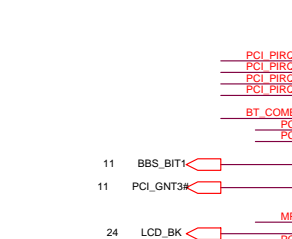
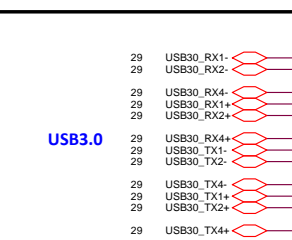
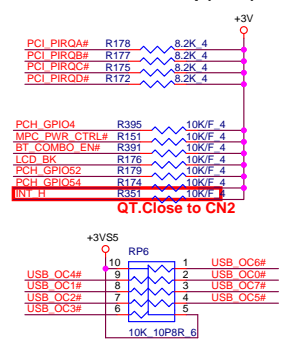
Vender	Size	P/N
AMIC	2MB	AKE38ZN0802 (A25LQ16M-F/Q)
GGD	2MB	AKE38GN0Q00 (GD25Q16BSIGR)



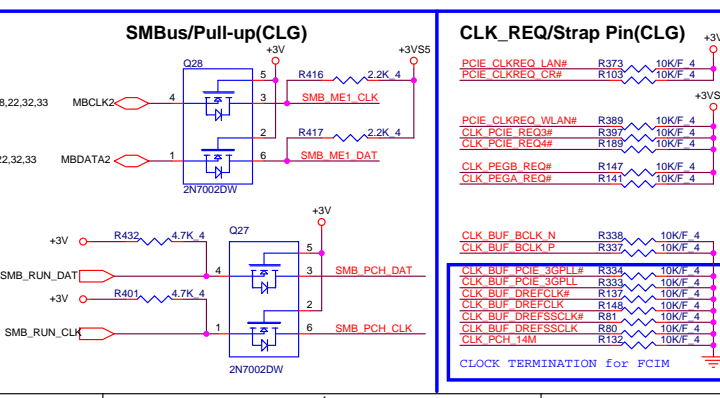
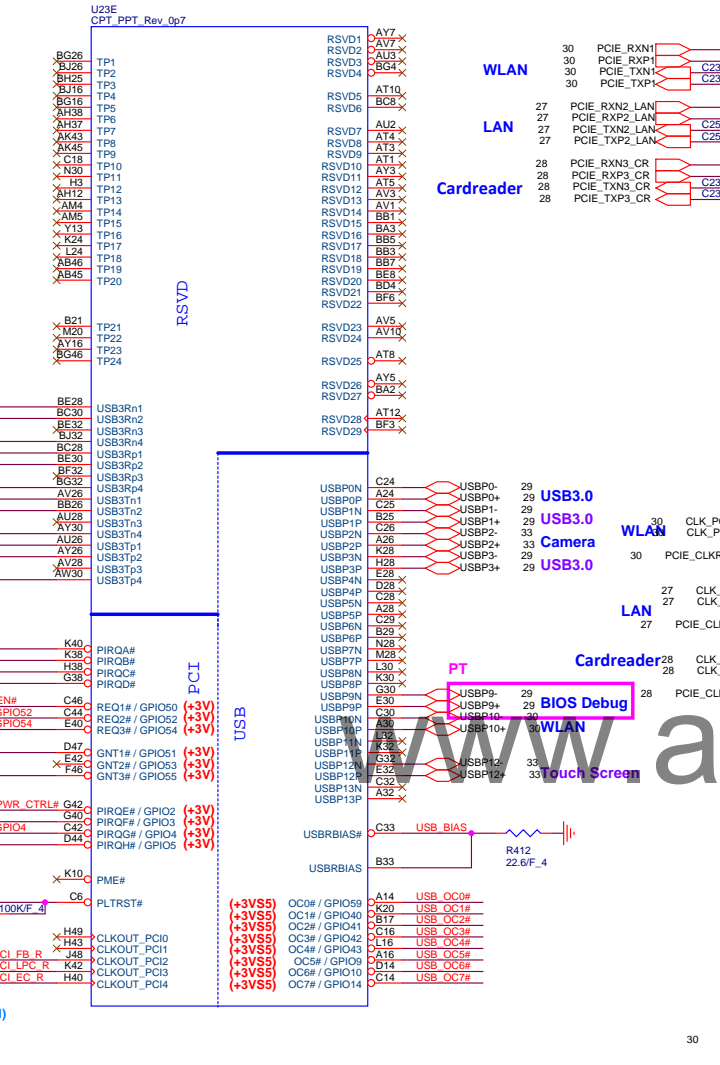
PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	Circuit						
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode							
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	+3V _{CC} 						
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V _{RTCC} 						
HDA_DOCK_EN#/GPIO33	Flash Descriptor Security Only for Interposer	PWROK	0 = Override 1 = Default (weak pull-up 20K)	 [Need external pull-down for LPC BIOS] Default weak pull-up on GNT0/1#						
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1" data-bbox="642 1131 875 1181"><thead><tr><th>GNT1#</th><th>GNT0#</th><th>Boot Location</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>SPI LPC</td></tr></tbody></table>	GNT1#	GNT0#	Boot Location	0	0	SPI LPC	
GNT1#	GNT0#	Boot Location								
0	0	SPI LPC								
GPIO19 Different from Calpella	Boot BIOS Selection 0 [bit-0]	PWROK		 BBS_BIT0 12						
GNT2# / GPIO53	ESL strap (Server only)	PWROK	Should not be pull-down (weak pull-up 20K)	USE GPIO PIN						
NV_ALE	Intel Anti-Theft HDD protection Only for Interposer	PWROK	0 = Disable (Internal pull-down 20kohm)							
NV_CLE	DMI Termination voltage	PWROK	weak pull-down 20kohm	+1.8V _{CC} 						
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	+3V _{SS} 						
HDA_SDO	Flash Descriptor Security	PWROK	0 = Override 1 = Default (weak pull-up 20K)	+3V _{SS} 						
GPIO8	Integrated Clock Chip Enable	RSMRST#	Should be pull-down (weak pull-up 20K)							
GPIO28 Different from Calpella	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)							
SPI_MOSI	iTPM function Disable	APWROK	0 = Default (weak pull-down 20K) 1 = Enable							

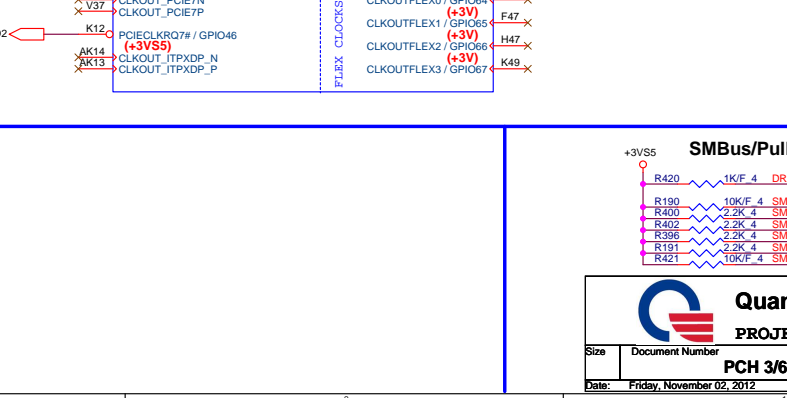
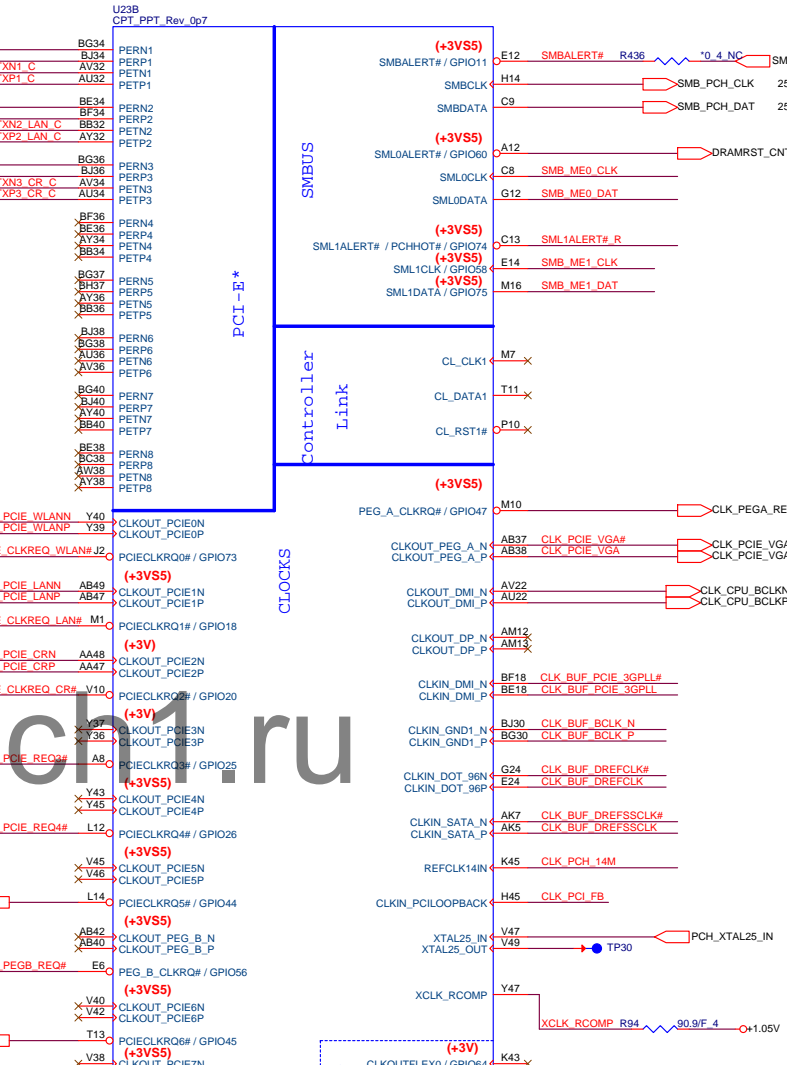
PCI/USBOC# Pull-up(CLG)



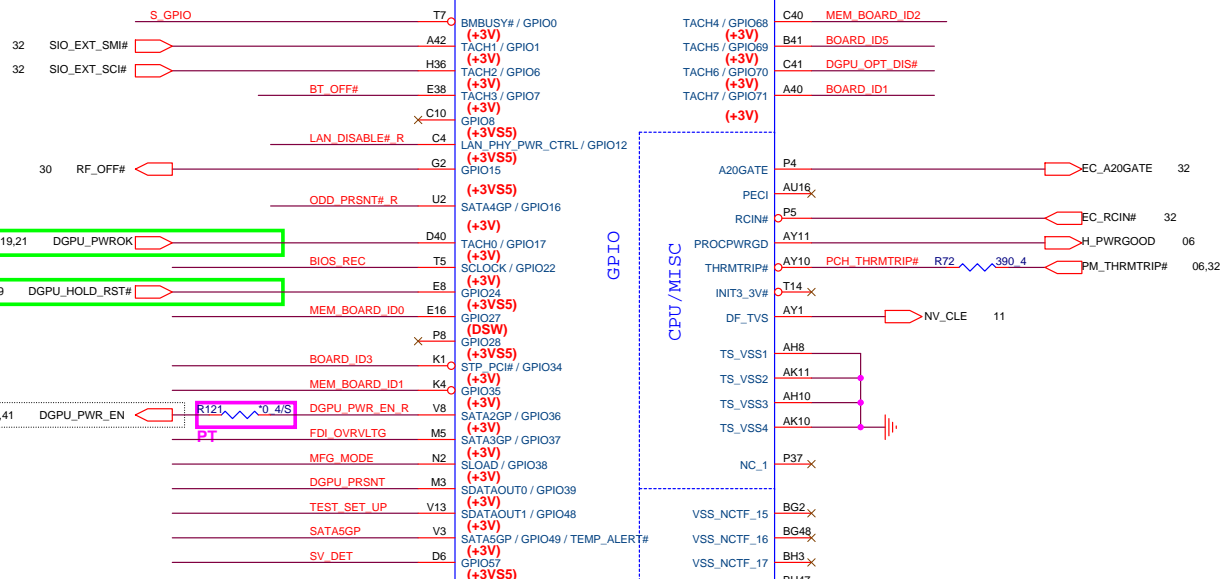
Cougar Point-M/Panther Point (PCI,USB,NVRAM)



Cougar Point-M/Panther Point (PCI-E,SMBUS,CLK)

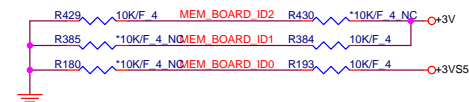


Cougar Point/Panther Point (GPIO,VSS_NCTF,RSVD)

U23F
CPT PPT Rev 0p7

OPTIMUS POWER control pin	
DGPU_PWROK	GPIO17
DGPU_HOLD_RST#	GPIO24
DGPU_PWR_EN	GPIO36

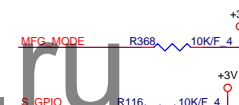
Default: HYNIX DDR3-1600 2GB



System Memory BOARD ID SETTING

	GPIO68 MEM_BOARD_ID2	GPIO35 MEM_BOARD_ID1	GPIO27 MEM_BOARD_ID0
HYNIX DDR3-1600 2GB	0	0	0
SAMSUNG DDR3-1600 2GB	0	0	1
On Board DDR3 N.C	0	1	1
RESERVE	0	1	0
RESERVE	1	0	0
RESERVE	1	0	1
RESERVE	1	1	1
RESERVE	1	1	0

MFG-TEST



Intel ME Crypto Transport Layer Security (TLS) cipher suite

Low = Disable (Default)
High = Enable

BIOS RECOVERY High = Disable (Default)
Low = Enable

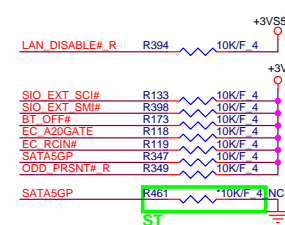
TEST SET_UP R102 10K/F 4

SV_SET_UP High = Strong (Default)

R152 100K/F 4 SV_DET

TEST DETECT Low = Default

GPIO Pull-up/Pull-down(CLG)



R138 100K/F 4 FDI_OVRVLGT

FDI TERMINATION VOLTAGE OVERRIDE Reserved only

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PROJECT : JW8

Size Document Number PCH 4/6 (GPIO) Rev 3A

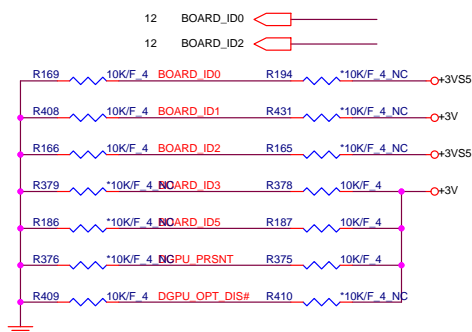
Date: Friday, November 02, 2012 Sheet 13 of 46

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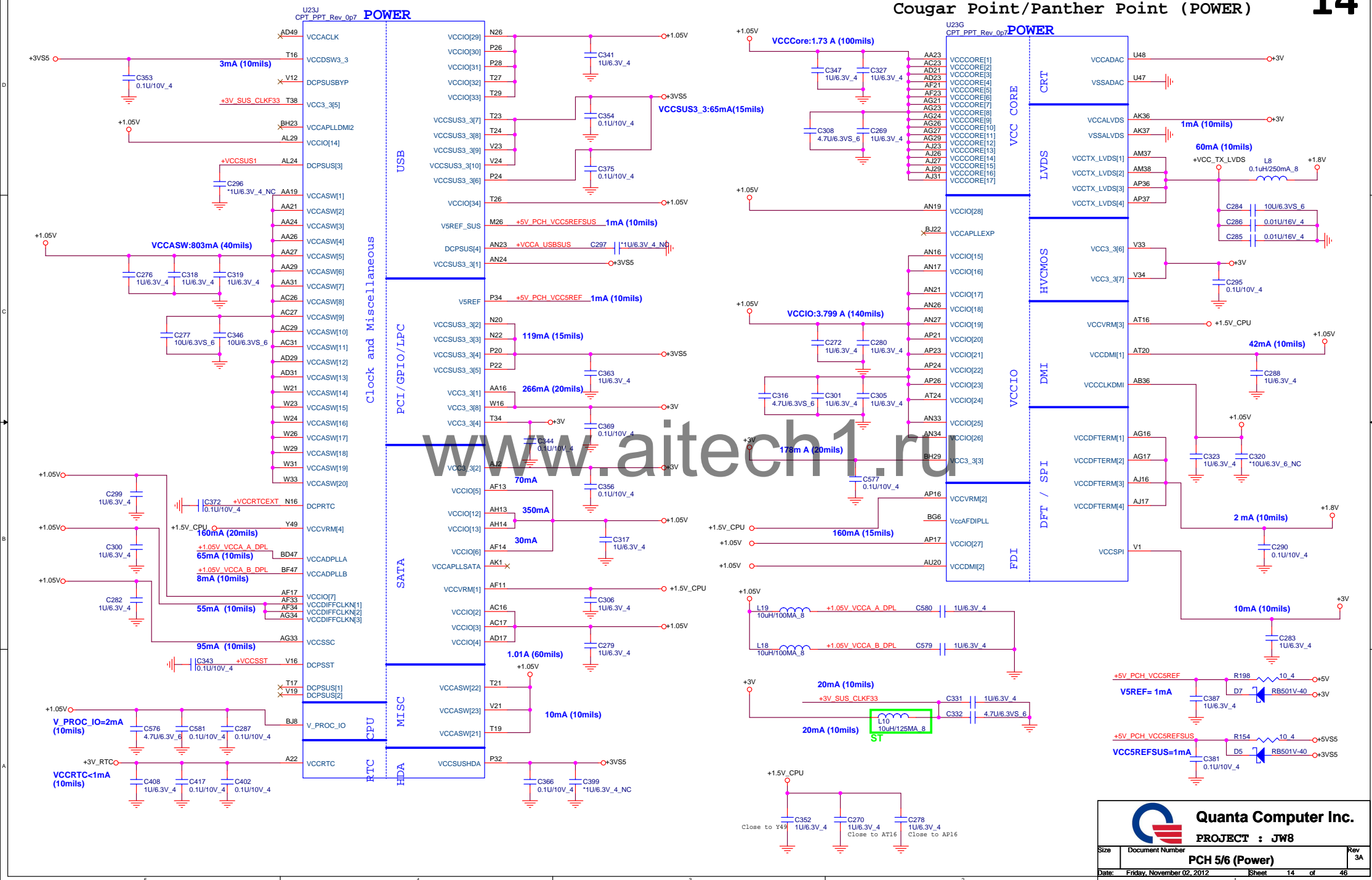
BOARD_ID[3:0]	Model Name
0000	ST2 SV nonTouch
0001	ST2 ULV nonTouch
0010	ST2 SV Touch
0011	ST2 ULV Touch
0100	QT SV nonTouch
0101	QT ULV nonTouch
0110	QT SV Touch
0111	QT ULV Touch
1000	ST1 SV nonTouch
1001	Reserve
1010	ST1 SV Touch
1011	Reserve

Chief River BOARD ID SETTING

BOARD_ID0	GPIO44	SV=0, ULV=1
BOARD_ID1	GPIO71	NonTouch=0, Touch=1
BOARD_ID2	GPIO46	Phase select
BOARD_ID3	GPIO34	Phase select
BOARD_ID5	GPIO69	HM76=0, HM77=1
DGPU_PRSTNT	GPIO39	Optimus=1, UMA=0
DGPU_OPT_DIS#	GPIO70	Optimus=0, Dis only=1



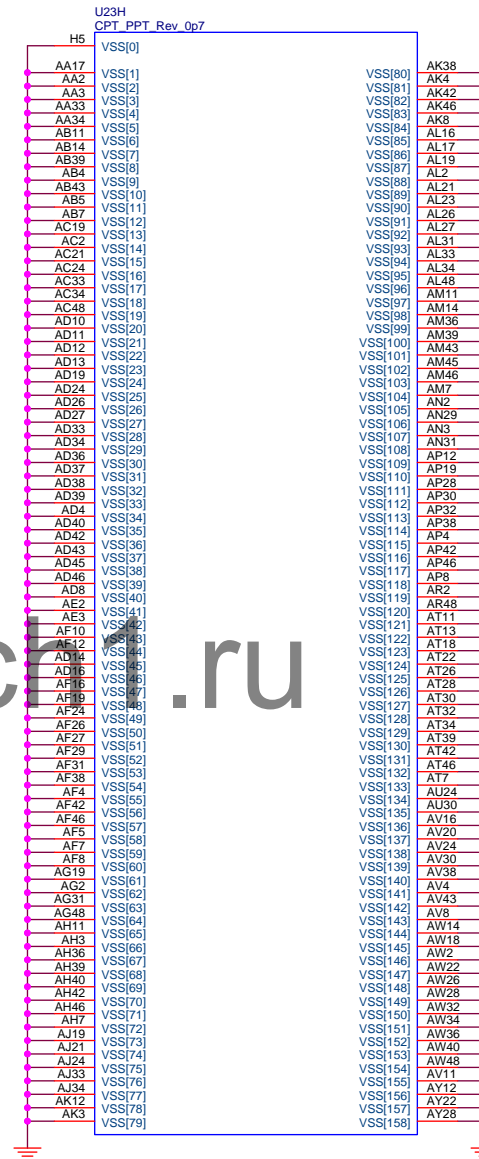
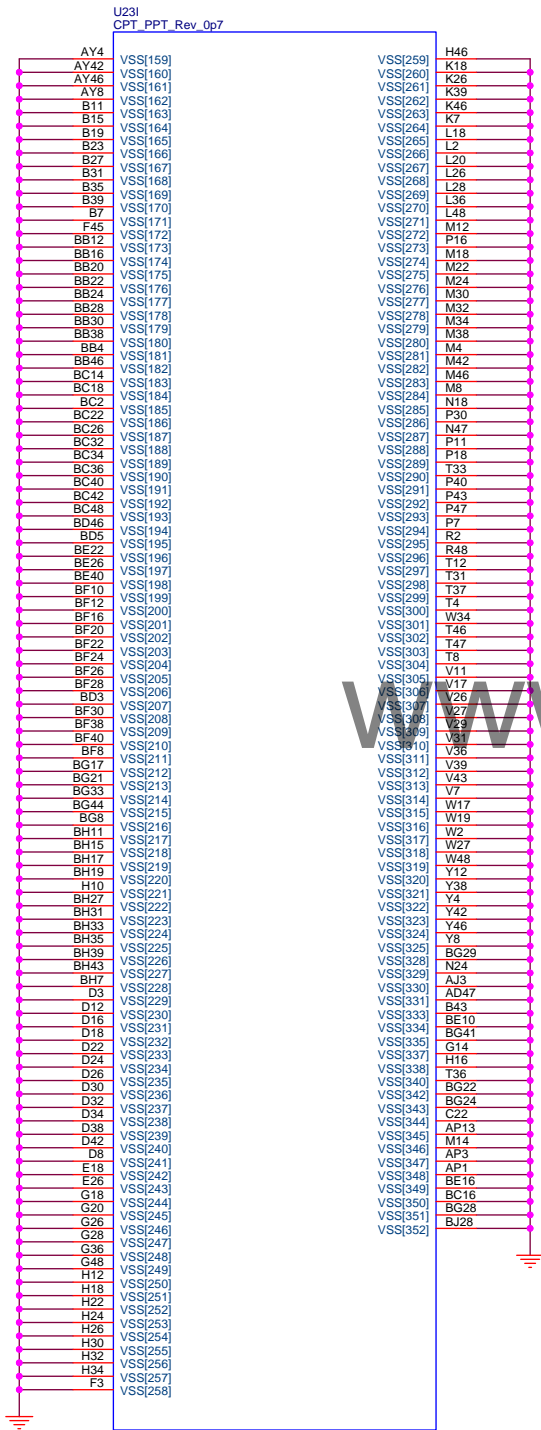
Cougar Point/Panther Point (POWER)



Cougar Point/Panther Point (GND)

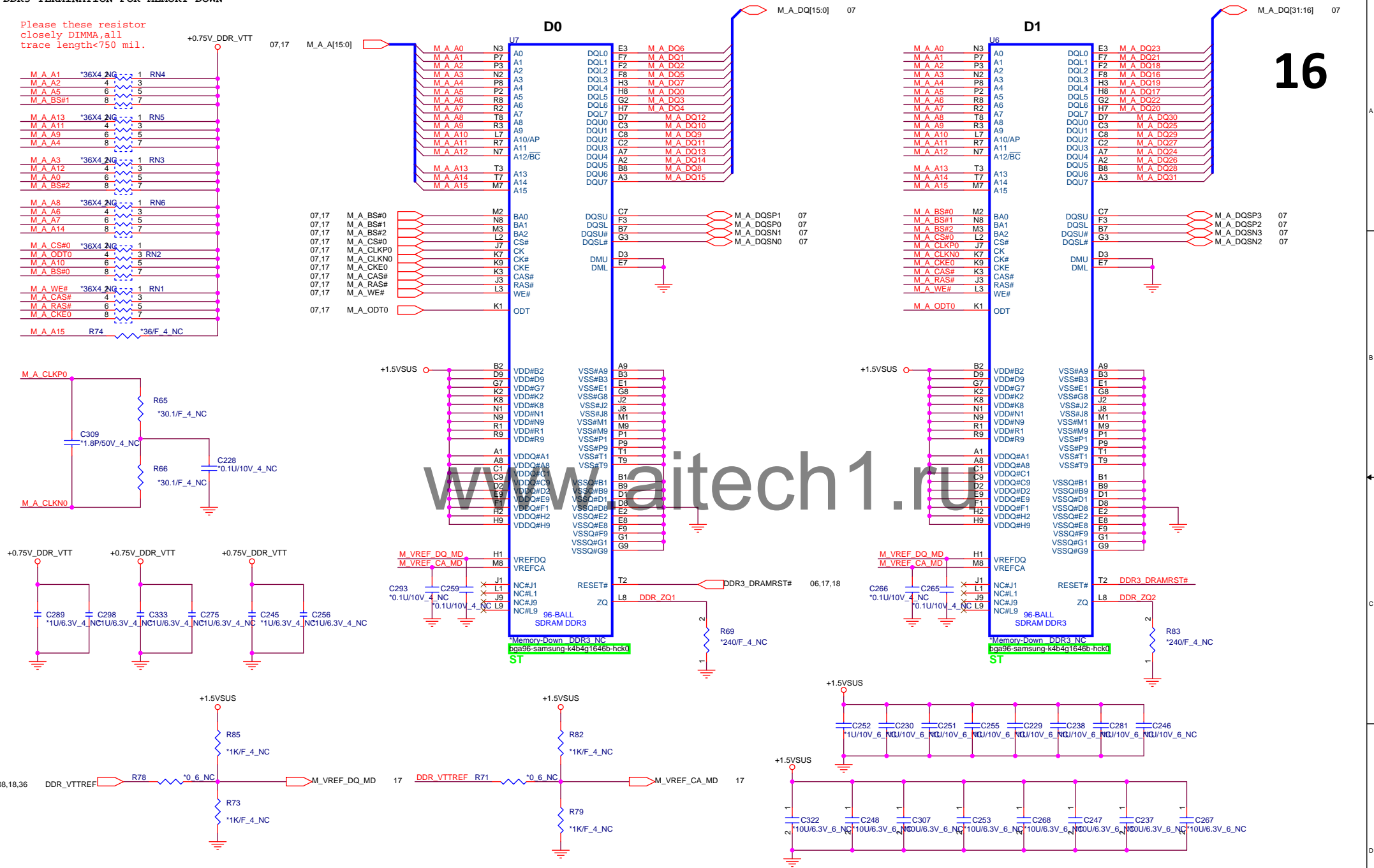
Cougar Point/Panther Point (GND)

15



DDR3 TERMINATION FOR MEMORY DOWN

Please these resistor
closely DIMMA,all
trace length<750 mil.





DDR3 Thermal Sensor

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm1.

+1.5VSUS

Capacitor	Value	Footprint
C241	1U/6.3V	4
C240	1U/6.3V	4
C212	1U/6.3V	4
C217	1U/6.3V	4
C209	4.7U/6.3VS	6
C215	4.7U/6.3VS	6
C213	4.7U/6.3VS	6
C242	4.7U/6.3VS	6
C214	4.7U/6.3VS	6
C239	4.7U/6.3VS	6
C210	*10U/6.3V	6 NC
C236	10U/6.3V	6
C208	10U/6.3V	6

+0.75V_DDR_VTT

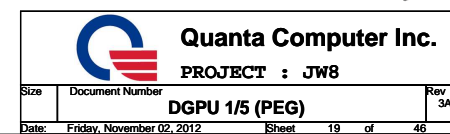
Capacitor	Value	Footprint
C202	1U/6.3V	4
C203	1U/6.3V	4
C218	1U/6.3V	4
C224	1U/6.3V	4
C221	4.7U/6.3VS	6
C226	*10U/6.3V	6 NC
C225	0.1U/10V	4
C227	2.2U/6.3V	6

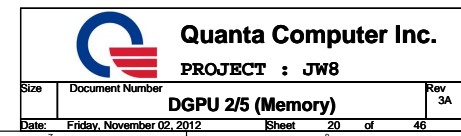
+3V

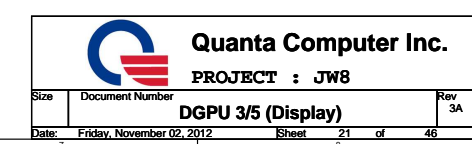
Capacitor	Value	Footprint
C207	0.1U/10V	4
C205	2.2U/6.3V	6
C216	0.1U/10V	4
C204	2.2U/6.3V	6

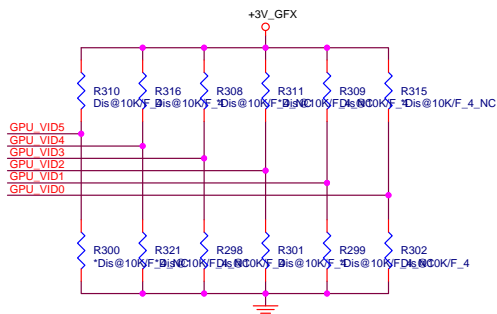
Capacitors C205 and C204 are highlighted with green boxes and labeled **ST**.

VREF DQ1 M1 Solution

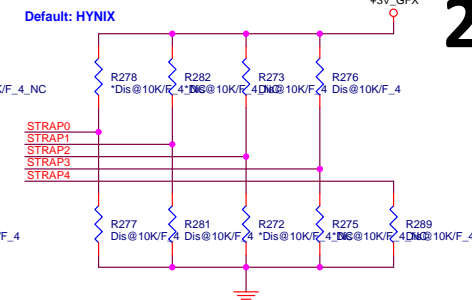
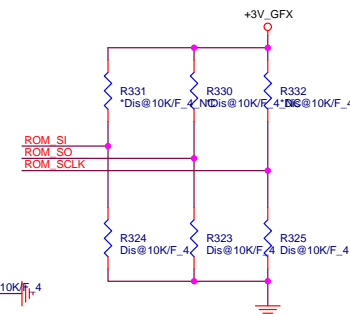
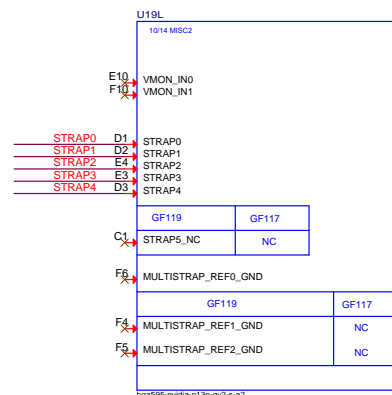








N13P-GV2 NVDD HW BOOT Voltage = 0.875V
VID = 110010



Binary Strap Mode Mapping

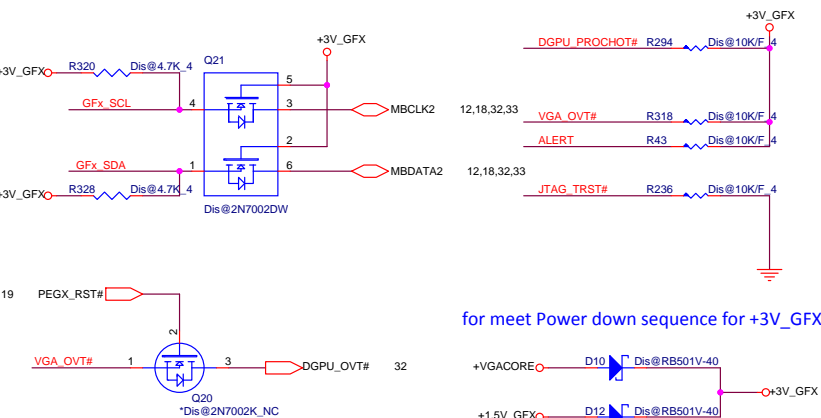
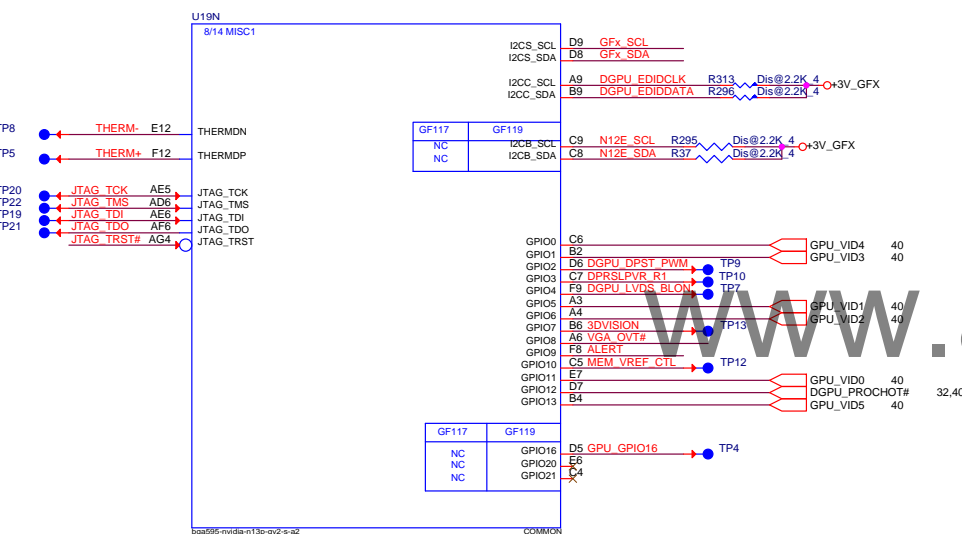
Strap Pin name	Strap Mapping	Resistance	Polarity
ROM_SCLK	SMB_ALT_ADDR	10Kohm	Pull-down to GND
ROM_SI	SUB_VENDOR	10Kohm	Pull-UP to 3V3 if VBIOS ROM Exists Pull-down to GND if no VBIOS ROM
ROM_SO	VGA_DEVICE	10Kohm	Pull-down to GND (no dispaly)
STRAP0	RAMCFG[0]	10Kohm	USER defined
STRAP1	RAMCFG[1]	10Kohm	USER defined
STRAP2	RAMCFG[2]	10Kohm	USER defined
STRAP3	RAMCFG[3]	10Kohm	USER defined
STRAP4	PCIE_MAX_SPEED	10Kohm	Pull-down to GND

VRAM Configuration Table

RAMCFG [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N	
0000		Reserved			
1100	DDR3 128Mx16x4, 64bit, 2Gb, 900MHz	HYNIX	H5TQ2G63DPR-11C	AKD5MGWTW16	
1011	DDR3 128Mx16x4, 64bit, 2Gb, 900MHz	SAMSUNG	K4W4G1646B-HC11	AKD5MGWTW16	
	DDR3 256Mx16x4, 64bit, 4Gb, 900MHz	HYNIX	H5TQ4G63MFR-11C	AKD5MGWTW04	
	DDR3 256Mx16x4, 64bit, 4Gb, 900MHz	SAMSUNG	K4W4G1646B-HC11	AKD5MGWT516	

GPIO ASSIGNMENTS

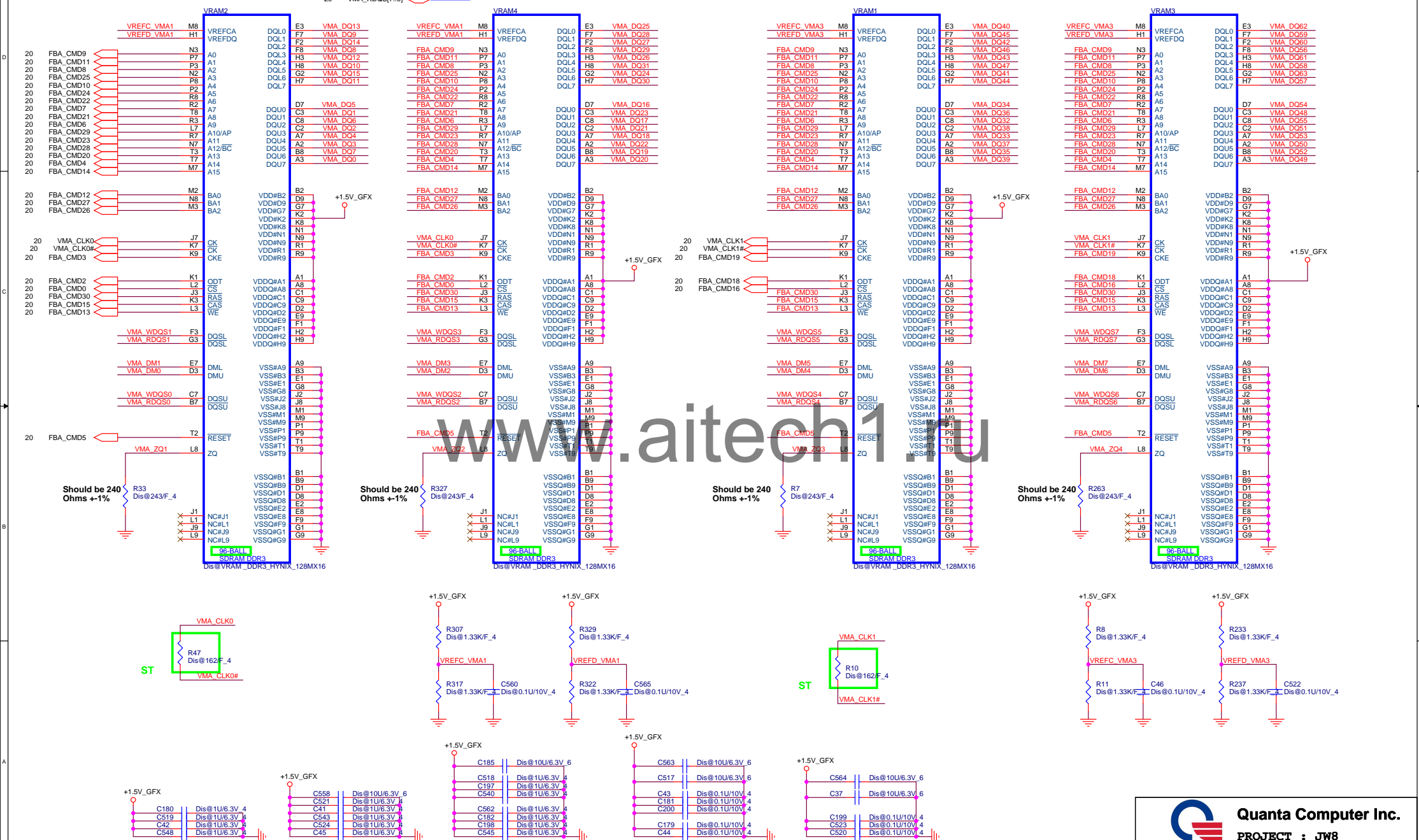
GPIO	I/O	PIN	USAGE
0	OUT	GPU_VID4	GPU CORE_VDD VID4
1	OUT	GPU_VID3	GPU CORE_VDD VID3
2	OUT	LCD_BL_PWM	LCD BACKLIGHT PWM
3	OUT	LCD_VCC	PANEL POWER ENABLE
4	OUT	LCD_BLEN	PANEL BACKLIGHT ENABLE
5	OUT	GPU_VID1	GPU CORE_VDD VID1
6	OUT	GPU_VID2	GPU CORE_VDD VID2
7	OUT	3D VISION	3D VISION LEFT/RIGHT VISION
8	I/O	OVERT	ACTIVE LOW THERMAL OVER TEMP
9	I/O	ALERT	ACTIVE LOW THERMAL ALERT
10	OUT	MEM VREF	MEMORY VREF CONTROL
11	OUT	GPU_VID0	GPU CORE_VDD VID0
12	IN	PWR_LEVEL	Power Detect ,HIGH=AC, LOW=DC
13	OUT	GPU_VID5	GPU CORE_VDD VID5
14	IN	HPD_AB	HOT PLUG DETECT FOR IFPAB
15	IN	HPD_C	HOT PLUG DETECT FOR IFPC
16	OUT	MEM_VDD	MEMMORY VDD CONTROL
17	IN	HPD_D	HOT PLUG DETECT FOR IFPD
18	IN	HPD_E	HOT PLUG DETECT FOR IFPE
19	IN	HPD_F	HOT PLUG DETECT FOR IFPF
20/21		RESERVE	

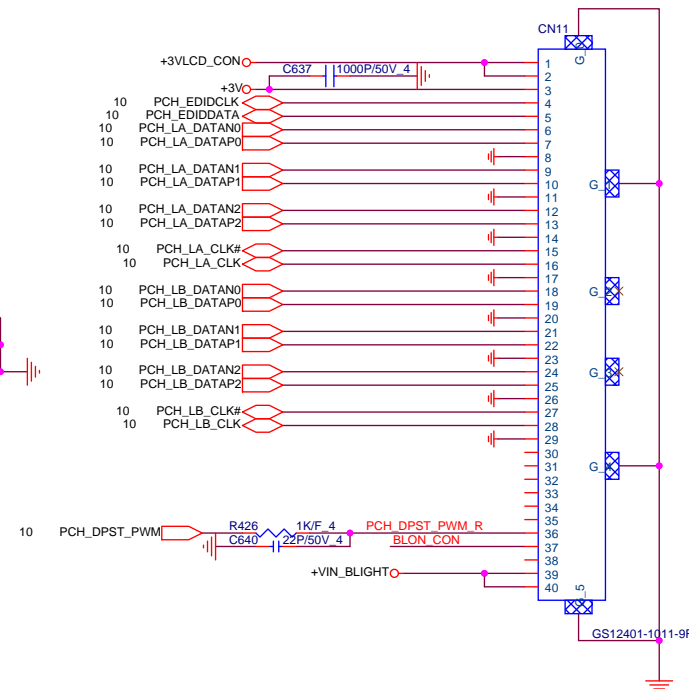


for meet Power down sequence for +3V_GFX

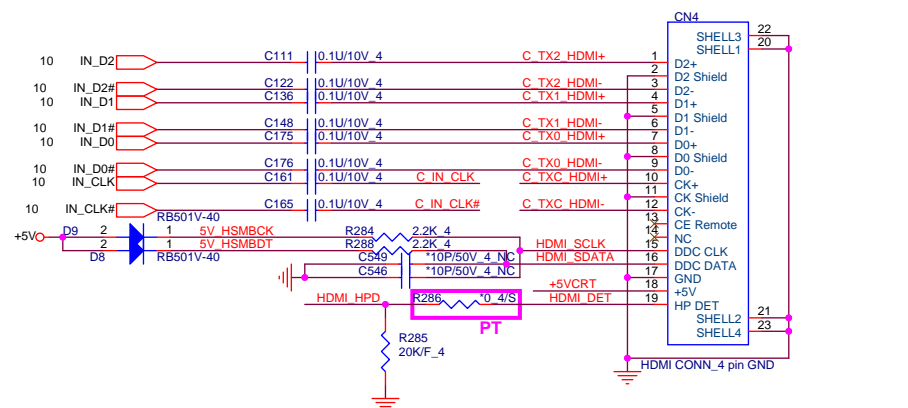
900MHz VRAM size:
 Samsung 256Mx16, P/N = AKD5MGWT516
 Samsung 128Mx16, P/N = AKD5MGWT520
 Hynix 256Mx16, P/N = AKD5PGWTW04
 Hynix 128Mx16, P/N = AKD5MGWTW16

CHANNEL A: 256MB/512MB DDR3

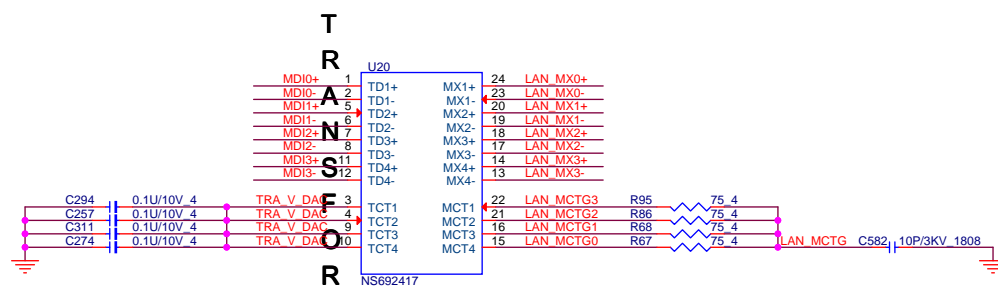
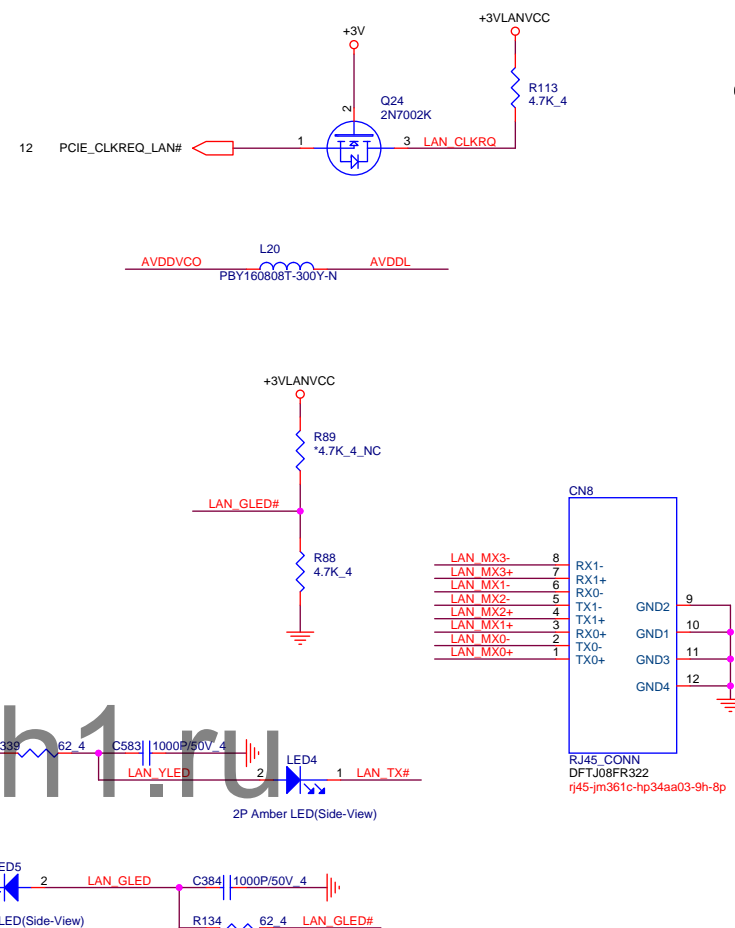
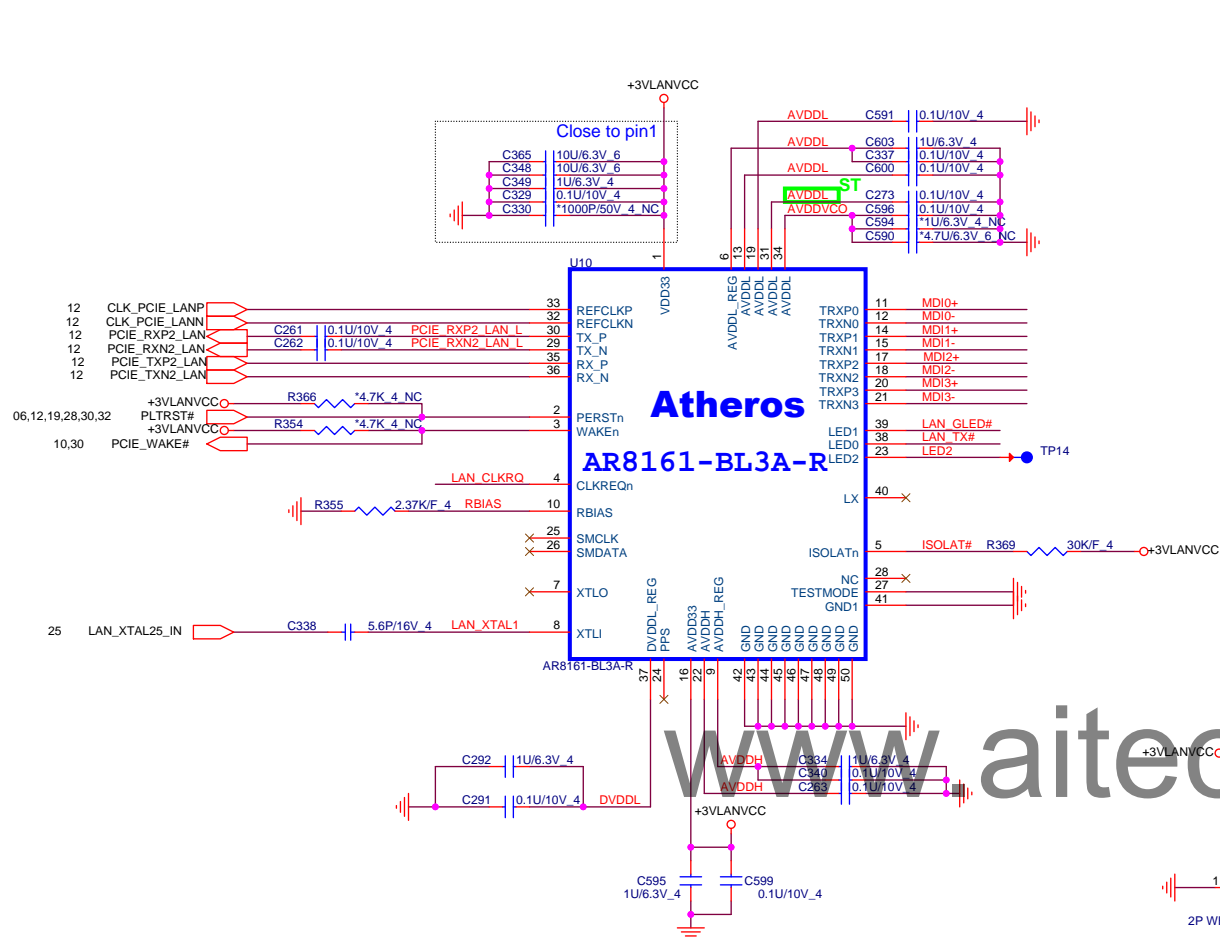




HDMI PORT



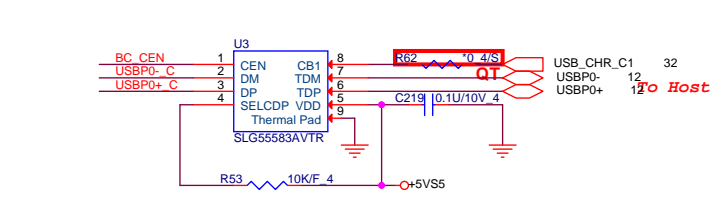




FCE: N692417, DB0KL3LAN02
BOT: NA0069R LF, DB0KL3LAN01

Charger USB

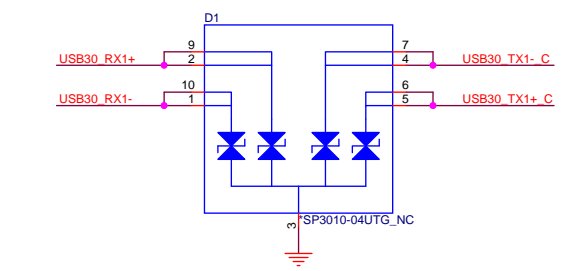
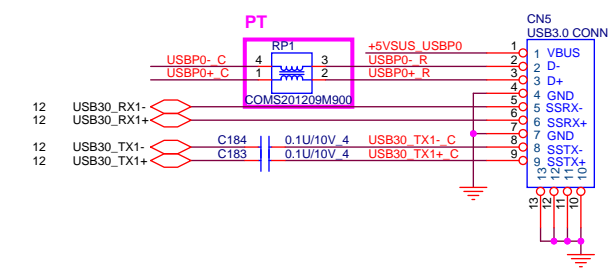
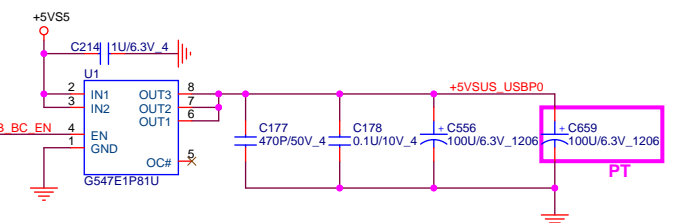
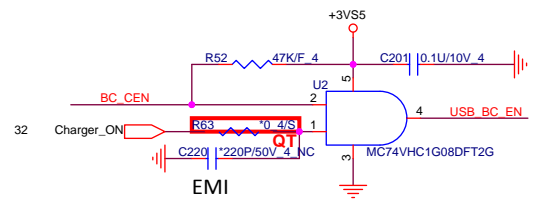
USB3.0/2.0 COMBO X 1 29



CB	SELCDP	Function
0	X	DCP autodetect with mouse/keyboard wakeup
1	0	S0 charging with SDP only
1	1	S0 charging with CDP or SDP only (depending on external device)

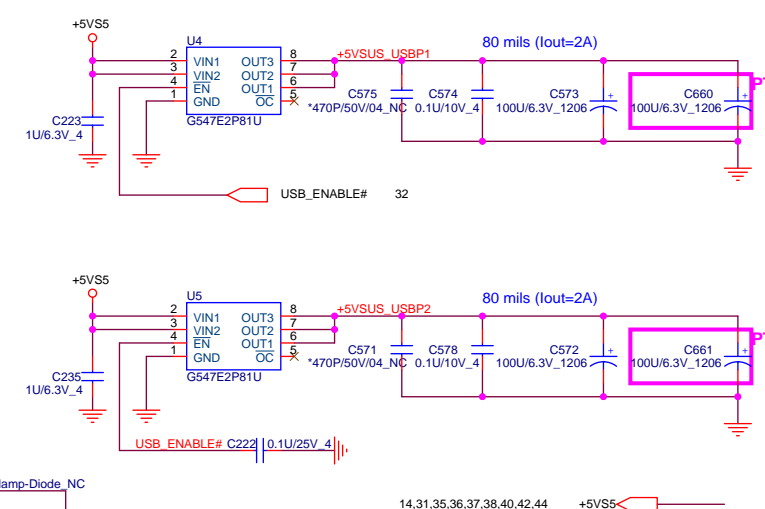
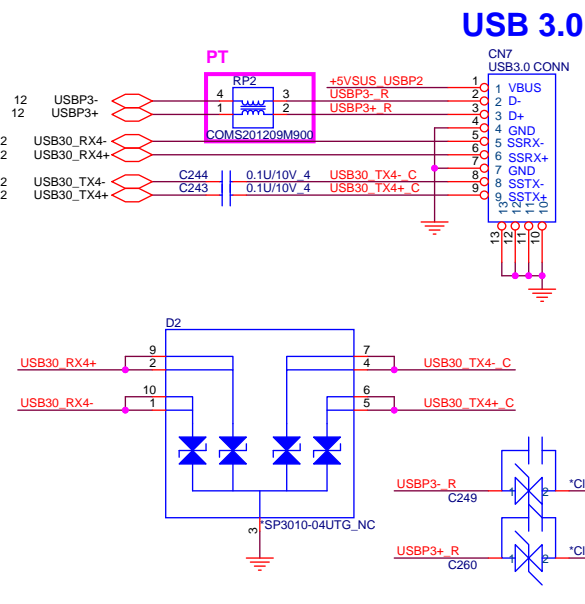
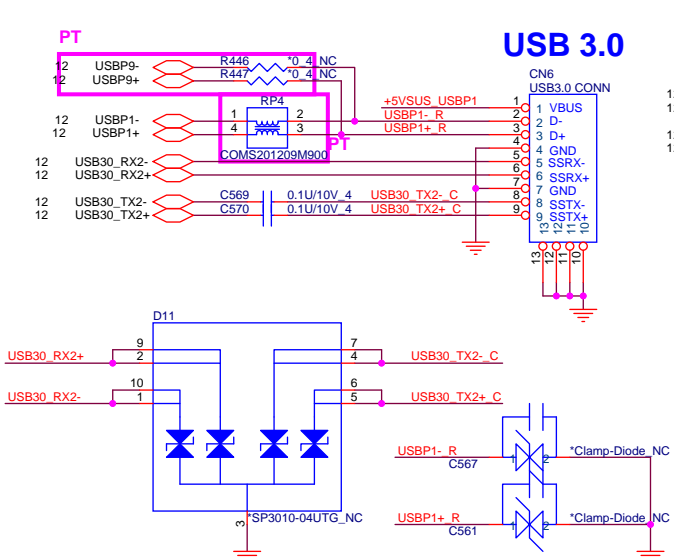
• USB Charge at S0 / S3 / S4 / S5 (Set by BIOS)

Current Battery Capacity	USB Charge (Set by BIOS)	S0		S3		S4/S5		EC wake up to read battery capacity from deep sleep mode	
		AC	DC	AC	DC	AC	DC		
> battery level (20%)	Enable	CDP	CDP	DCP	DCP	DCP	DCP	No	Yes
	Disable (Default)	CDP	CDP	Off	Off	Off	Off	No	No
<= battery level (20%)	Enable	CDP	CDP	DCP	Off	DCP	Off	No	No
	Disable (Default)	CDP	CDP	Off	Off	Off	Off	No	No

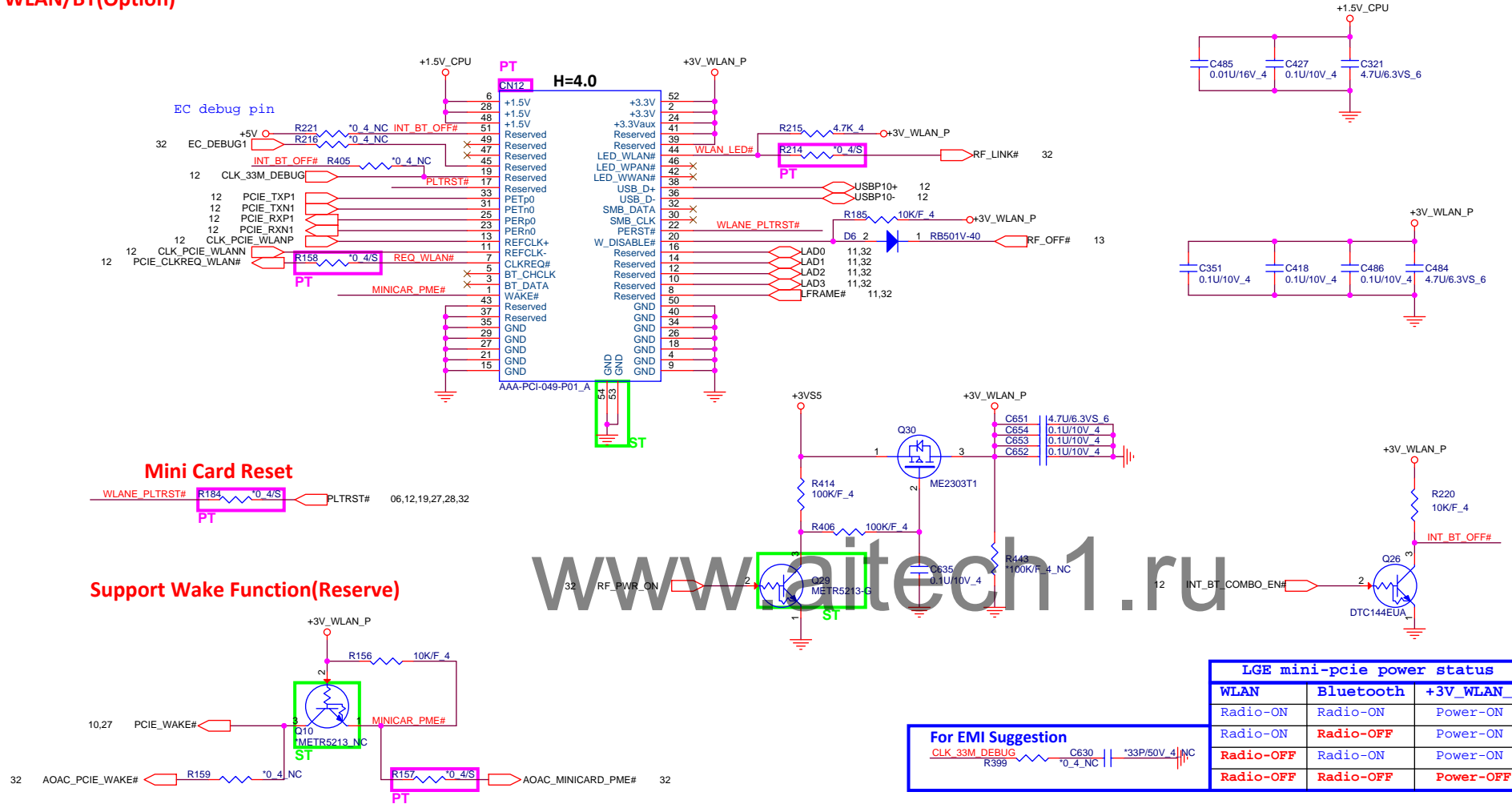


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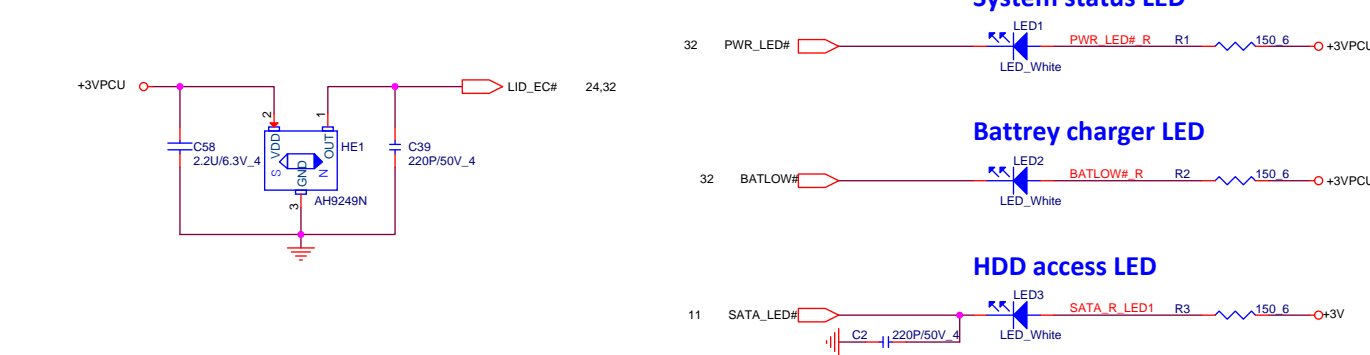
USB3.0/2.0 COMBO X 2



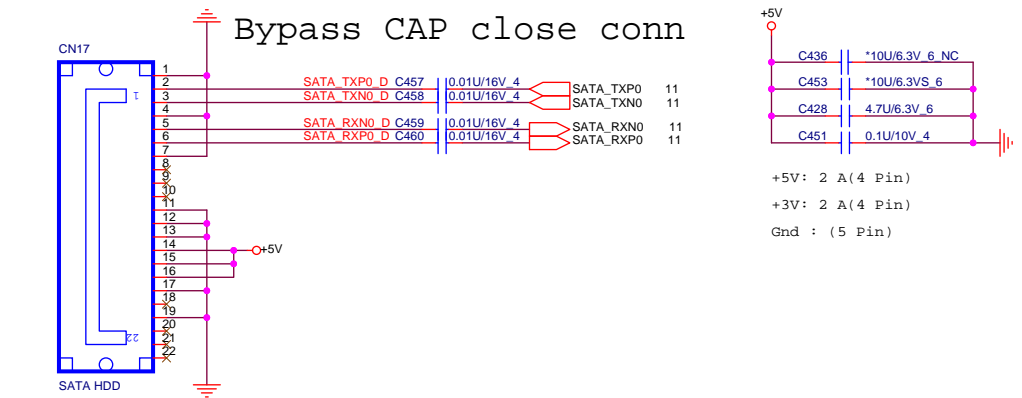
Mini Card
WLAN/BT(Optional)



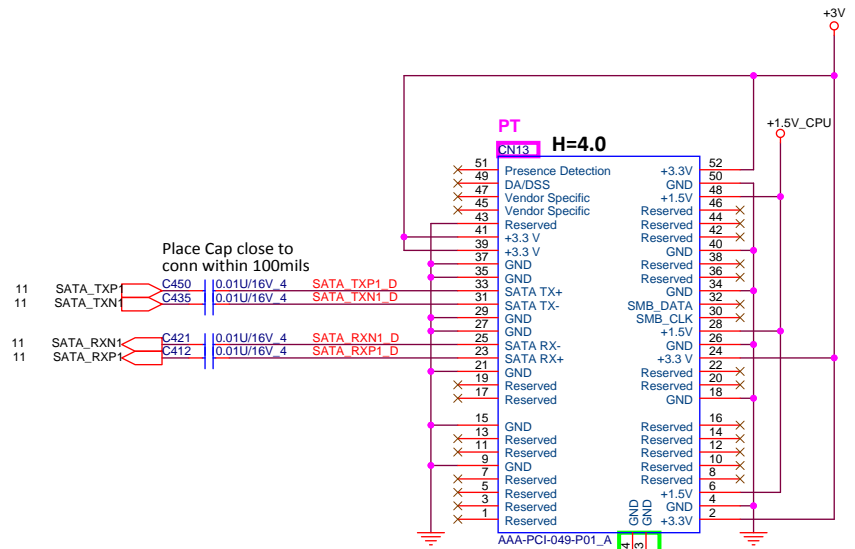
LED Status



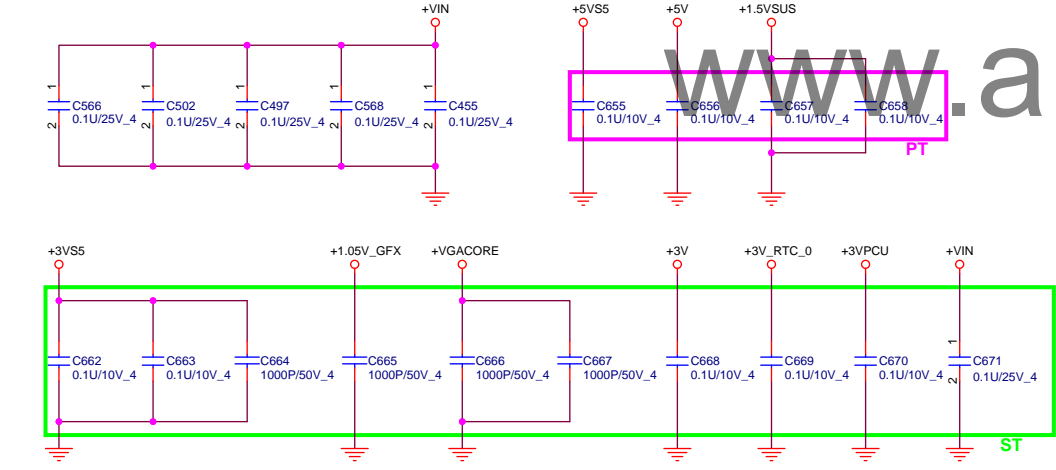
SATA HDD Connector

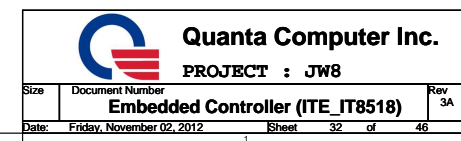


mSATA



EMI

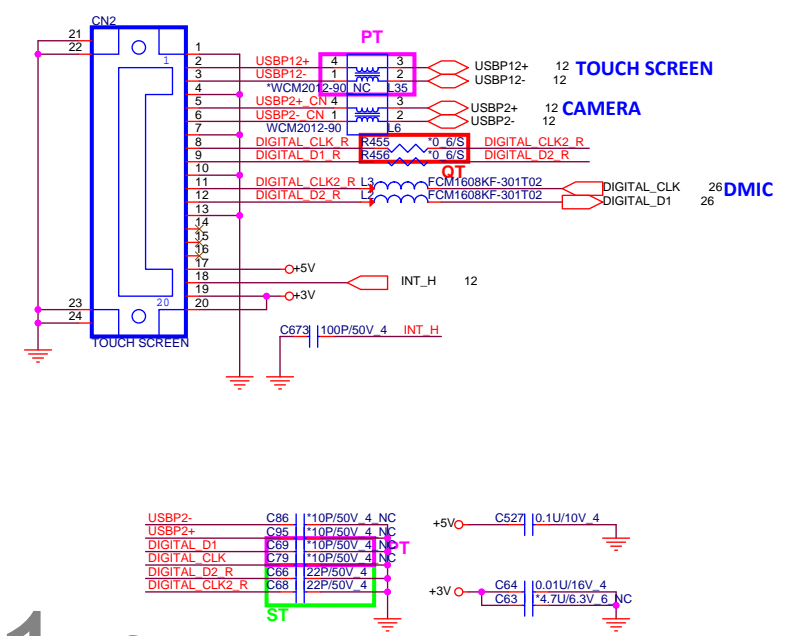
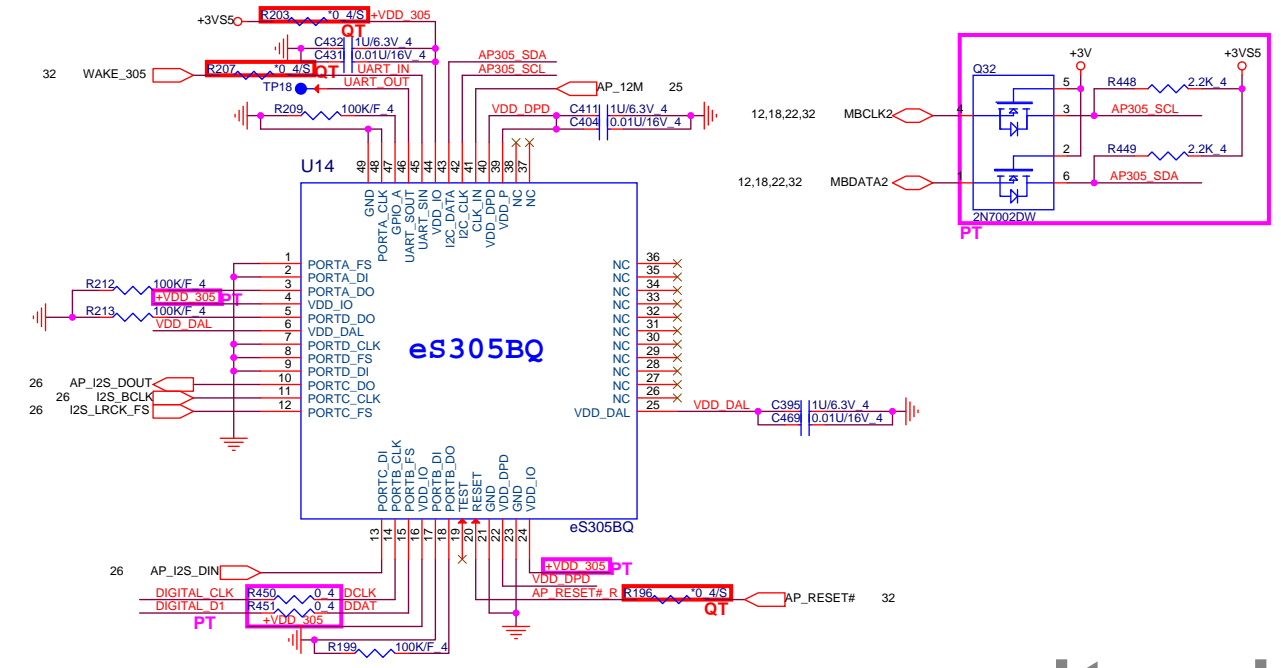




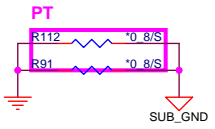
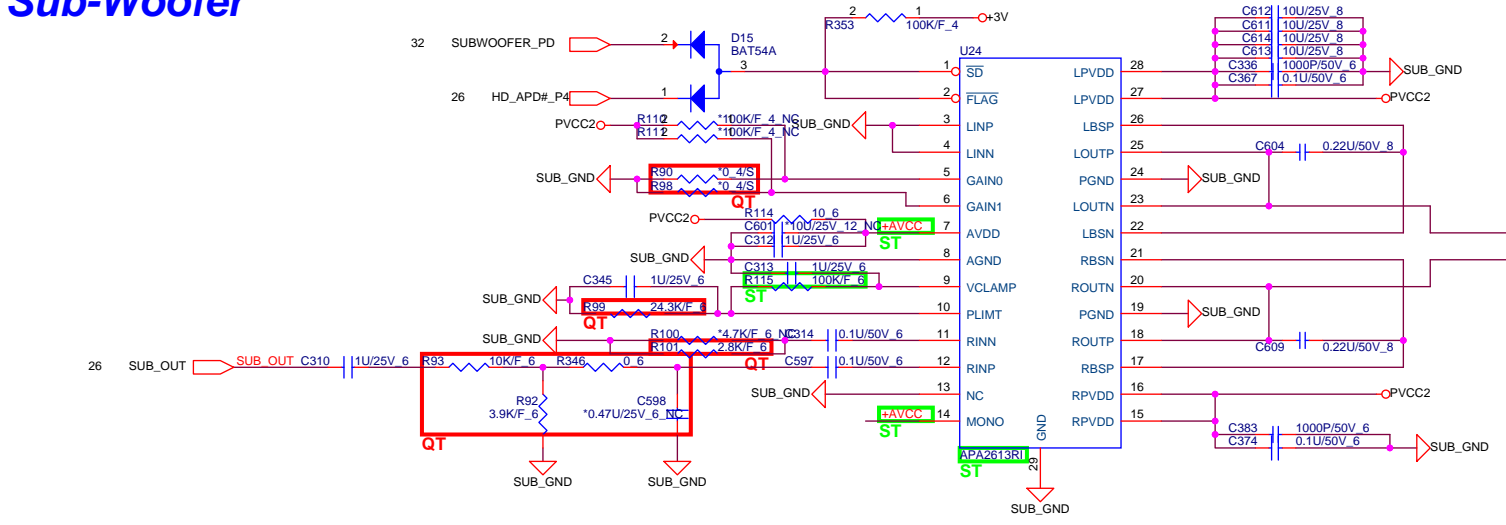
Audio Processor

Sub-Woofer

Touch Screen



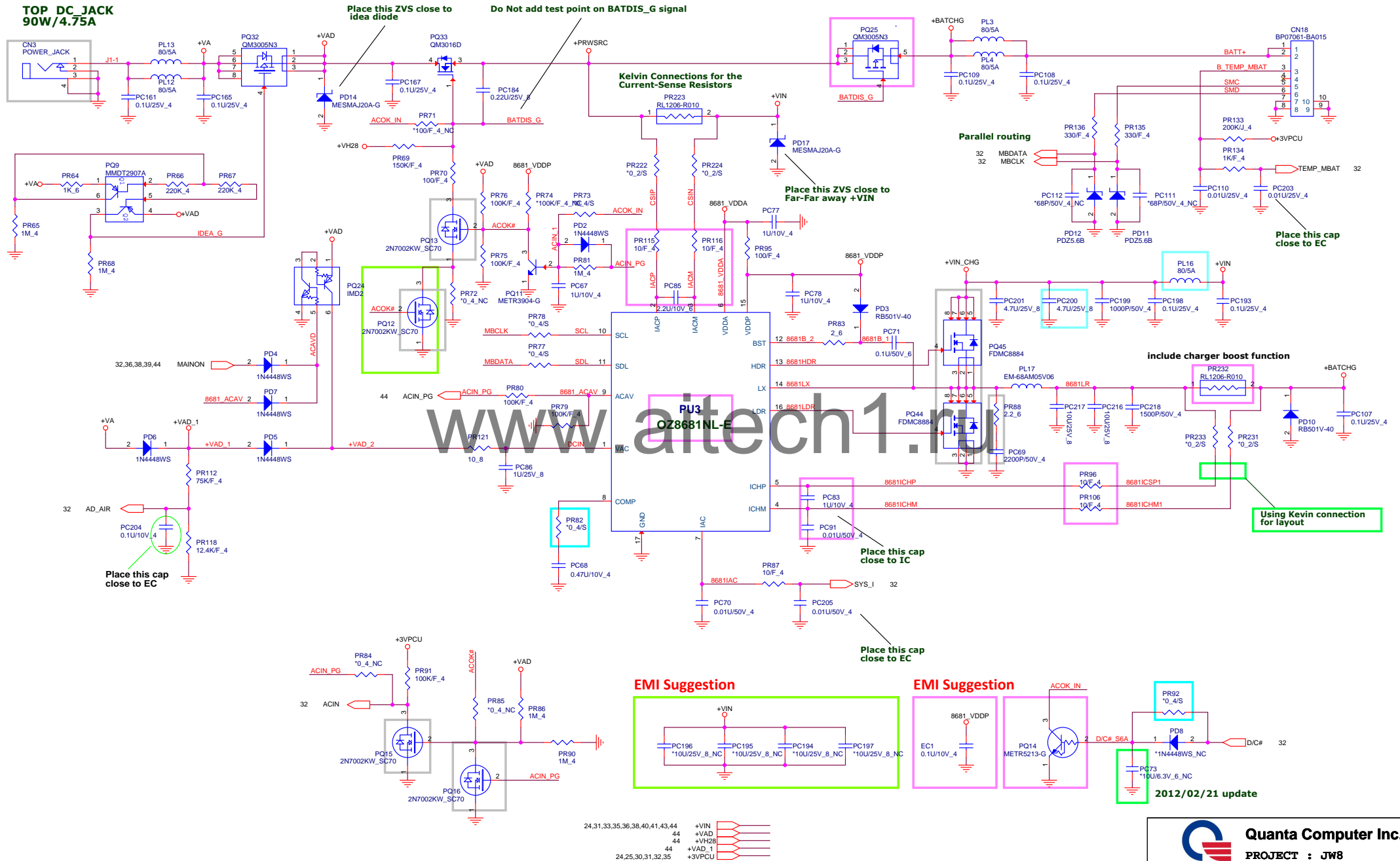
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GAIN1	GAIN0	dB
0	0	20
0	1	26
1	0	32
1	1	36

ANC: APA2613RI-TRG, AL002613K00
TIC: TPA3111D1PWPR, AL003111K00

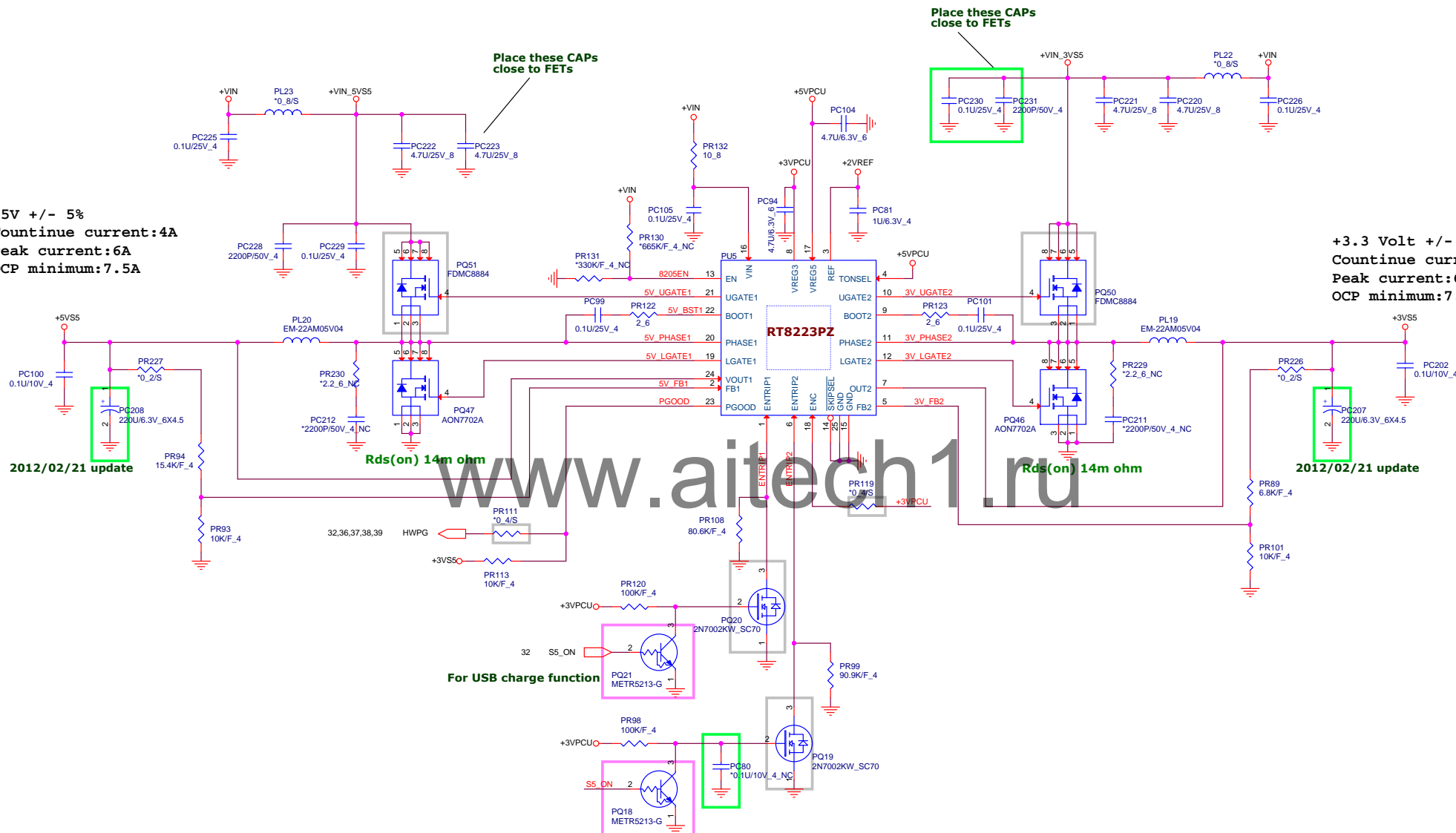
TOP DC JACK 90W/4.75A



24,31,33,35,36,38,40,41,43,44
44 +VIN
44 +VAD
44 +VH28
44 +VAD_1
44 +3VPCU

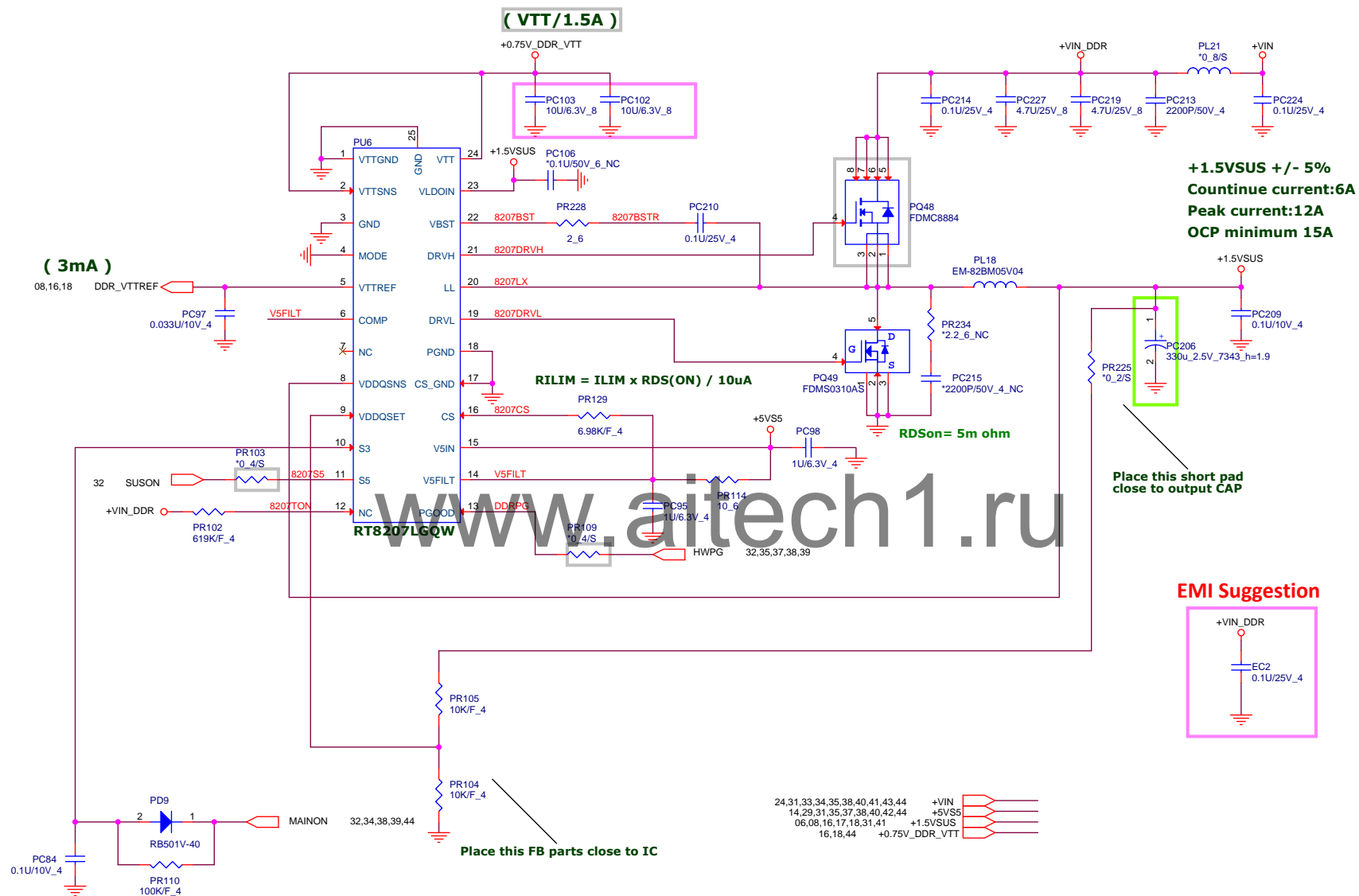
+5V +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A

+3.3 Volt +/- 5%
Countinue current:4A
Peak current:6A
OCP minimum:7.5A



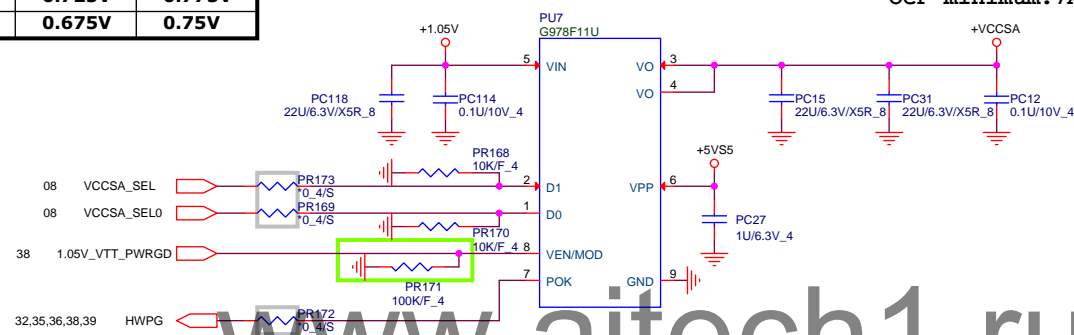
24,31,33,34,36,38,40,41,43,44
 10,11,12,13,14,25,29,30,31,32,33,38,39,41,44
 14,29,31,36,37,38,40,42,44
 24,25,30,31,32,34

+VIN
 +3VSS
 +5VSS
 +3VPCU



D0	D1	SV +VCCSA	ULV +VCCSA
0	0	0.9V	0.9V
0	1	0.8V	0.85V
1	0	0.725V	0.775V
1	1	0.675V	0.75V

+VCCSA Volt +/- 5%
 Countinue current:4A
 Peak current:6A
 OCP minimum:7A



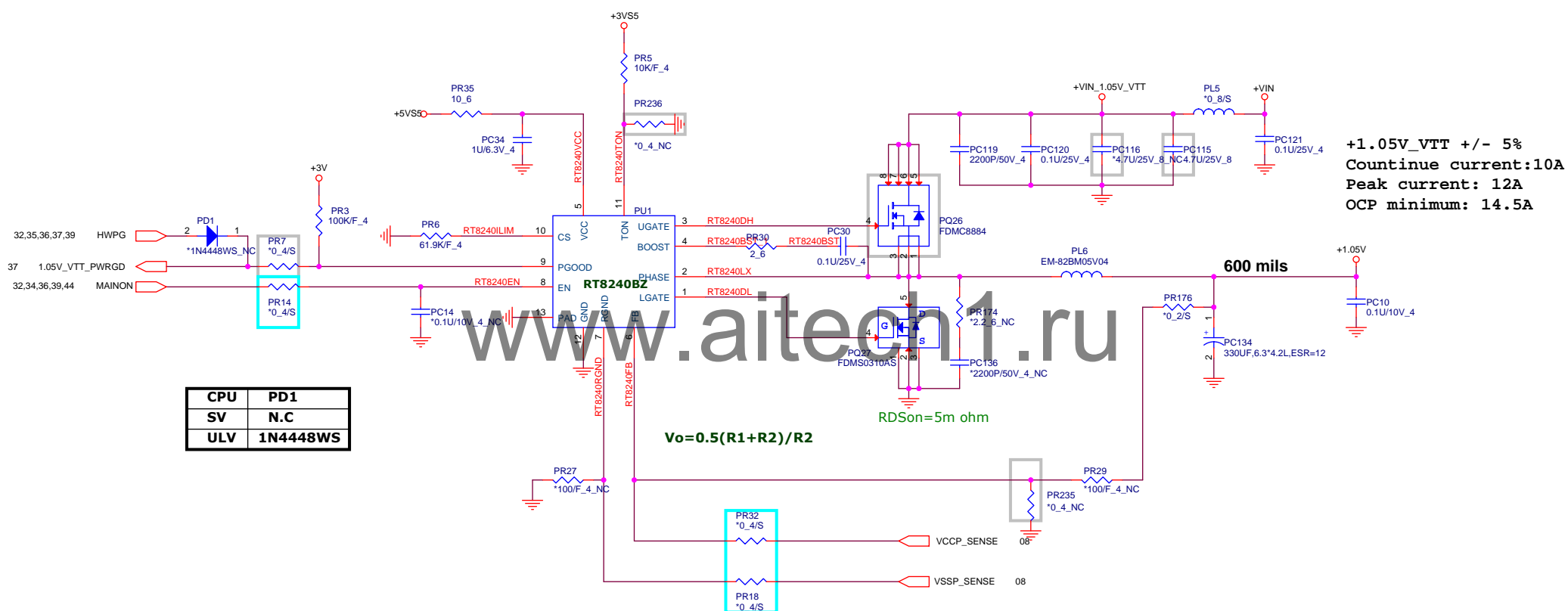
CPU	PR171
SV	100K/F_4
ULV	N.C



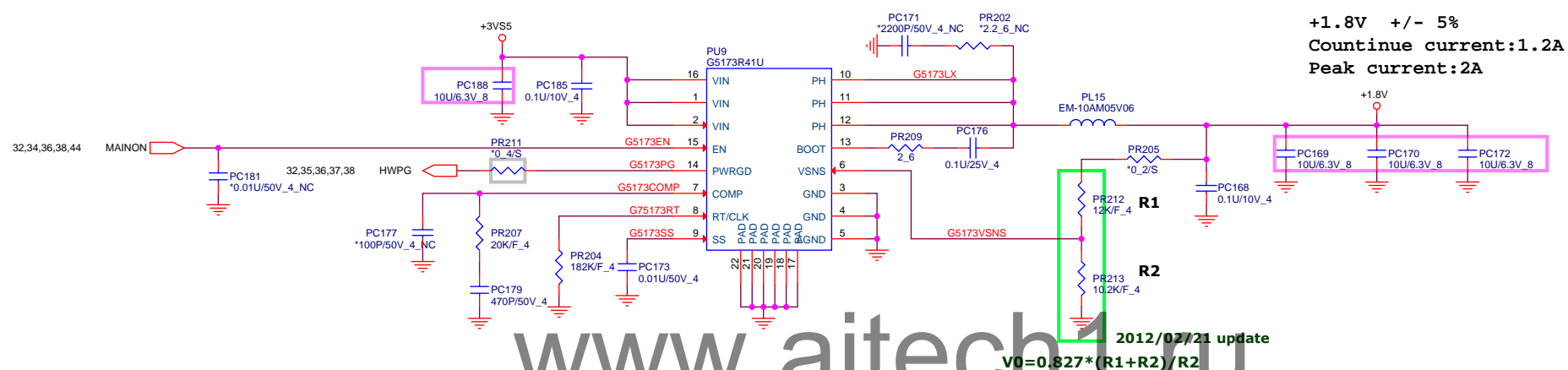
Quanta Computer Inc.

PROJECT : JW8

Size	Document Number	Rev
	+VCCSA (TPS51462RGER)	3A
Date:	Friday, November 02, 2012	Sheet 37 of 46



Quanta Computer Inc.
PROJECT : JW8



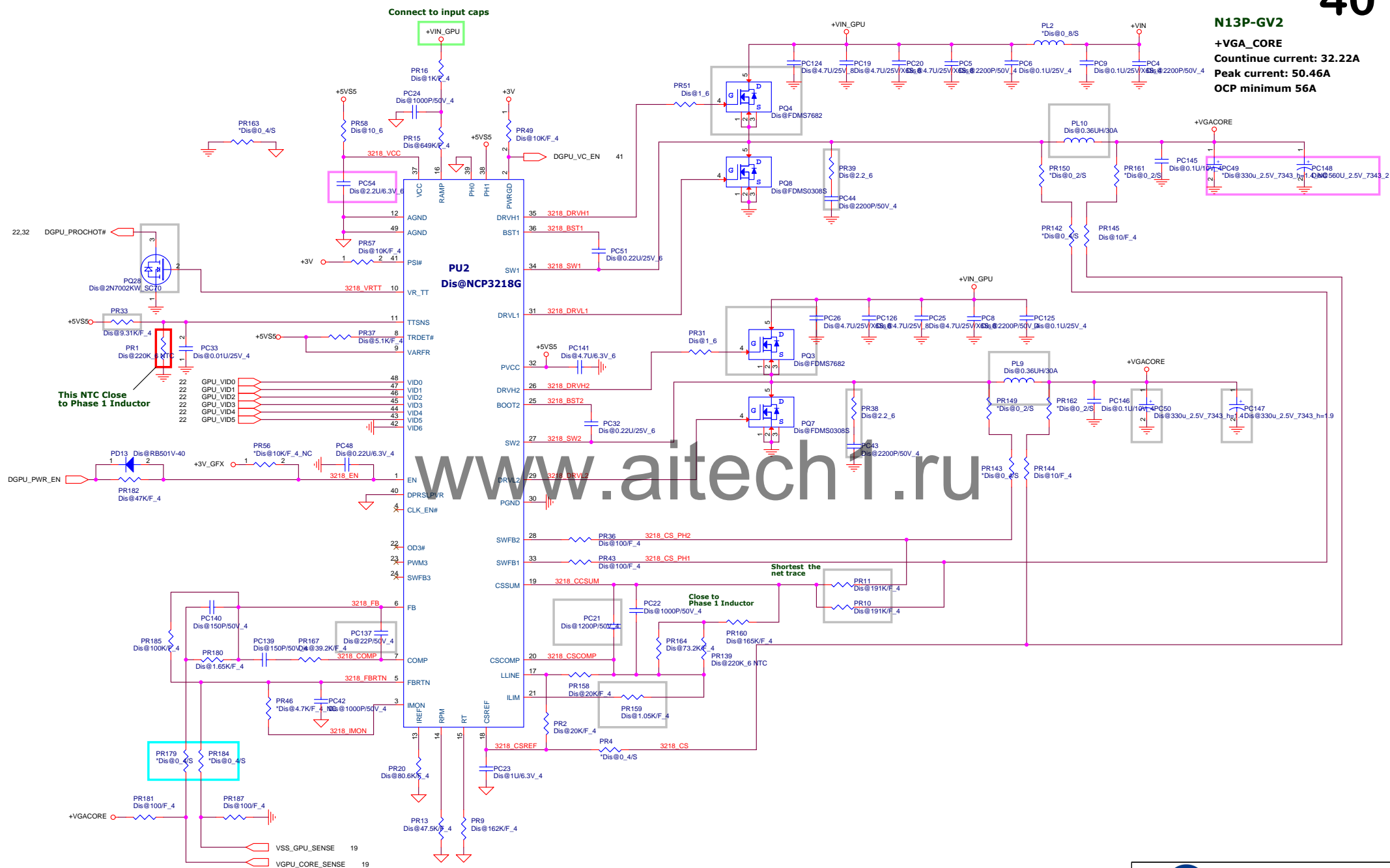
Quanta Computer Inc.

PROJECT : JW8

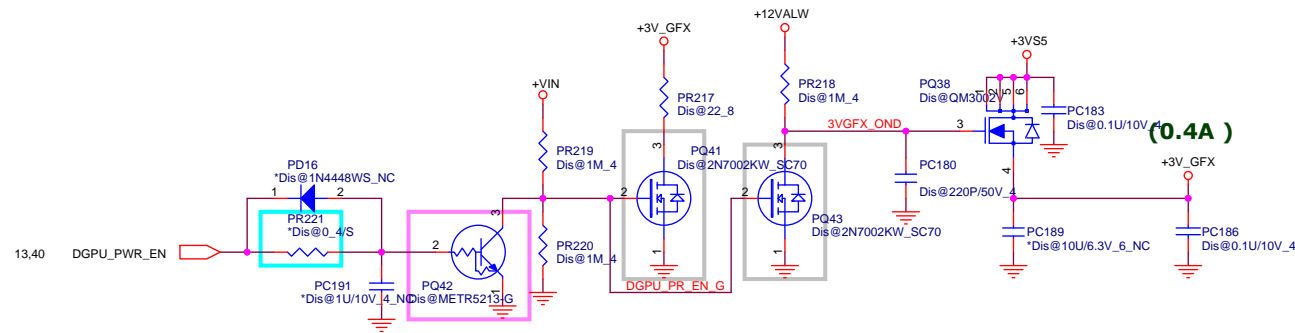
Size	Document Number	Rev
	+1.8V (G9661)	3A
Date:	Friday, November 02, 2012	Sheet 39 of 46

N13P-GV2

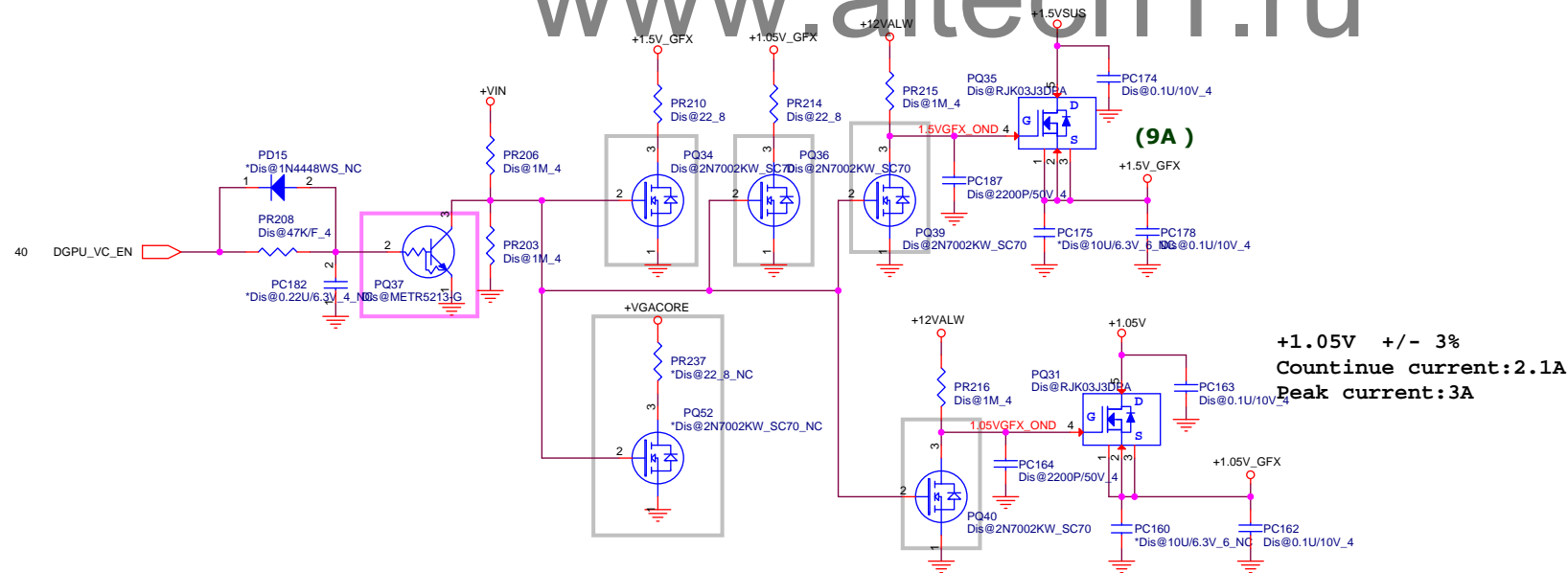
+VGA_CORE
Continue current: 32.22A
Peak current: 50.46A
OCP minimum 56A



06,08,16,17,18,31,36 +1.5VSUS
 10,11,12,13,14,25,29,30,31,32,33,35,38,39,44 +3VS5
 19,21,22,40 +3V_GFX
 20,21,22,23 +1.5V_GFX
 19,20,21,31 +1.05V_GFX
 44 +12VALW
 06,08,10,11,12,14,25,32,37,38,42 +1.05V



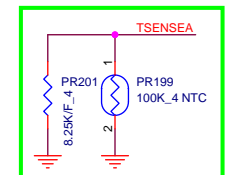
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Quanta Computer Inc.

PROJECT : JW8

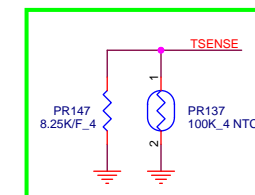
Size	Document Number	Rev
	+VGA POWER	3A
Date:	Friday, November 02, 2012	Sheet 41 of 46



Place NTC close with
V_GT hot spot

ULV Mode N.C

PR25, PC36, PC142, PR8



Place close with VCORE hot spot

POP Rc
For CPU 1PHASE only
operation

+VCC_CORE (ULV 17W)

TDC : 25A

Peak current: 33A

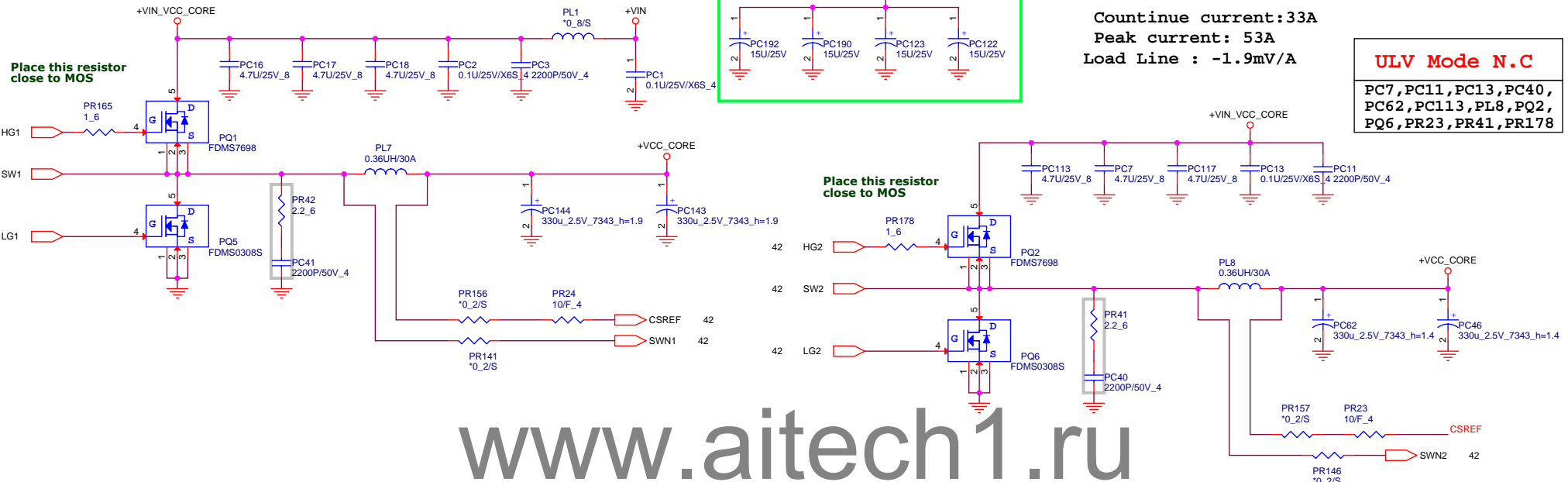
Load Line : -2.9mV/A

Countinue current:33A

Peak current: 53A

Load Line : -1.9mV/A

ULV Mode N.C

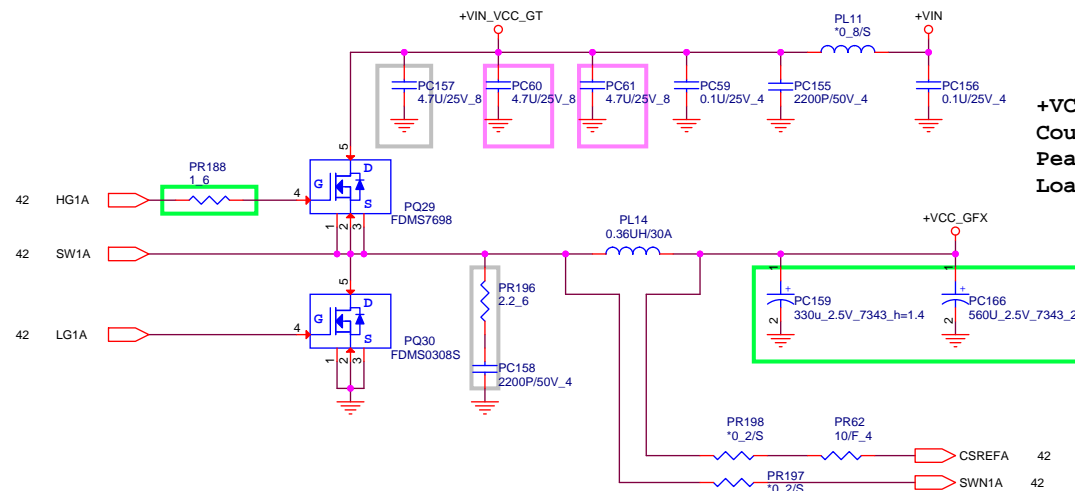
PC7,PC11,PC13,PC40,
PC62,PC113,PL8,PQ2,
PQ6,PR23,PR41,PR178

+VCC_GFX

Countinue current:21.5A

Peak current: 33A

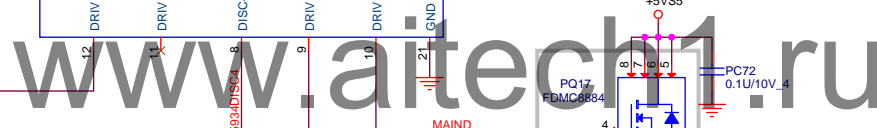
Load Line : -3.9mV/A



Quanta Computer Inc.

PROJECT : JW8

Size	Document Number	Rev
	CPU Core2 (NCP5911)DC	3A
Date	Friday, November 02, 2012	Sheet 43 of 46



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